SONY

CCD B/W VIDEO CAMERA MODULE

# XC-73/73CE
# XC-75/75CE

JUNCTION BOX
**JB-77**

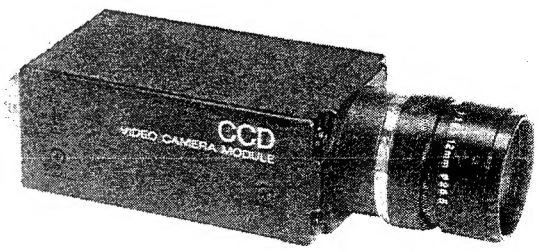
STANDARD LENS
**VCL-08YM**
**VCL-12YM**
**VCL-16Y-M**

TRIPOD ATTACHMENT
**VCT-37**

6-PIN M CONNECTOR
**PC-XC06**

12-PIN F CONNECTOR
**PC-XC12**

CAMERA CABLE
**CCXC-12P02/12P05**
**CCXC-12P10/12P25**
**CCXC-12P05D/12P05R**
**CCXC-12P05U/12P05S**




SERVICE MANUAL

XCM-7573

## SAFETY RELATED COMPONENT WARNING

**Components identified by shading and ⚠ marked on the schematic diagrams and parts list are critical to safe operation. Replace these components with SONY parts whose part numbers appear as shown in this manual or in supplements published by SONY.**

**For the customers in the USA**

**WARNING**

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

You are cautioned that any changes or modifications not expressly approved in this manual could void your authority to operate this equipment.

The shielded interface cable recommended in this manual must be used with this equipment in order to comply with the limits for a digital device pursuant to Subpart B of Part 15 of FCC Rules.

**For the customers in Canada**

This apparatus complies with the Class A limits for radio noise emissions set out in Radio Interference Regulations.

**Pour les utilisateurs au Canada**

Cet appareil est conforme aux normes Classe A pour bruits radioélectriques, spécifiés dans le Règlement sur le brouillage radioélectrique.

**Bescheinigung des Herstellers**

Hiermit wird bescheinigt, daß das CCD-Videokameramodul XC-75CE in Übereinstimmung mit den Bestimmungen der Amtsblattverfügung Nr. 1046/1984 funkentstört ist.
Der Deutschen Bundespost wurde das Inverkehrbringen dieses Gerätes angezeigt und die Berechtigung zur Überprüfung der Serie auf Einhaltung der Bestimmungen eingeräumt.
Sony Corporation

**Hinweis**

Gemäß dem Amtsblatt des Bundesministers für das Post- und Fernmeldewesen Nr. 163/1984 wird der Betreiber darauf aufmerksam gemacht, daß die von ihm mit diesem Gerät zusammengestellte Anlage auch den technischen Bestimmungen dieses Amtsblattes genügen muß.

**Bescheinigung des Herstellers/Importeurs**

Hiermit wird bescheinigt, daß das CCD-Videokameramodul XC-73CE in Übereinstimmung mit den Bestimmungen der BMPT-Amtsblatt Vfg 243/1991, Vfg 46/1992 funkentstört ist.
Der vorschriftsmäßige Betrieb mancher Geräte (z.B.Meßsender) kann allerdings gewissen Einschränkungen unterliegen. Beachten Sie deshalb die Hinweise in der Bedienungsanleitung.
Dem Bundesamt für Zulassungen in der Telekommunikation wurde das Inverkehrbringen dieses Gerätes angezeigt und die Berechtigung zur Überprüfung der Serie auf Einhaltung der Bestimmungen eingeräumt.

| | |
|---|---|
| Name und Anschrift des Herstellers/Importeurs: | Sony Deutschland GmbH<br>Hugo Eckener Str. 20<br>D-5000 Köln 30 |

**Hinweis**

Gemäß dem Amtsblätter des BMPT Nrn. 61/1991 und 6/1992 wird der Betreiber darauf aufmerksam gemacht, daß die von ihm mit diesem Gerät zusammengestellte Anlage auch den technischen Bestimmungen dieser Amtsblätter genügen muß.

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# SECTION 1
# OPERATION

## 1-1. Overview

The XC-73/73CE is a monochrome video camera module using a CCD (Charge Coupled Device) solid state image sensor.

### High image quality

The CCD provides a high-resolution image with 768 × 494 pixels (XC-73) or 752 × 582 pixels (XC-73CE).

### Range of operating modes

You can easily select the required operating mode. The gain, for example, can be set to AGC (A), or to fixed gain (F) or manual gain control (M) by an external switch.
* $\gamma$ (gamma) compensation can be switched on or off by an internal jumpers.By an internal jumper connection to switch the charge accumulation mode from frame to field, if external sync signals in noninterlace mode are input, the same sensitivity can be obtained as in interlace mode.

* The internal switch is mounted instead of internal jumpers in the following serial number for the camera module.
Serial number ;
XC-73 (UCJ) : 10001 - 15550
XC-73CE (EK) : 400001 - 405150

### External synchronization

The camera module can be synchronized with three types of signals explained below. The capture frequency range is ±1% of the horizontal scan frequency.
HD (horizontal drive), VD (vertical drive) signals: The camera module automatically determines whether to operate in interlace or noninterlace mode from the HD and VD signals input for external synchronization.
VS (Video/Sync) signals: External synchronization with a video or composite sync signal. (The unit switches automatically between HD/VD and VS synchronization.)
Reset pulse signal: The timing for reading out the contents of the register can be adjusted by the reset pulse signal.

### Internal sync signal output

FLD (Field Index) signals are output constantly from the 6-pin connector. An internal switch change allows the HD and VD signals also to be output from the 12-pin connectors.

### Electronic shutter function

Shutter speed can be selected from a wide range (1/125 to 1/10000 sec.) or in flickerless (FL) mode.

### Body fixing

Two mounting screw holes are provided in the reference plane on the lower surface of the body, allowing mounting with the absolute minimum deviation of the optical axis.

### Compatibility with the series XC-77

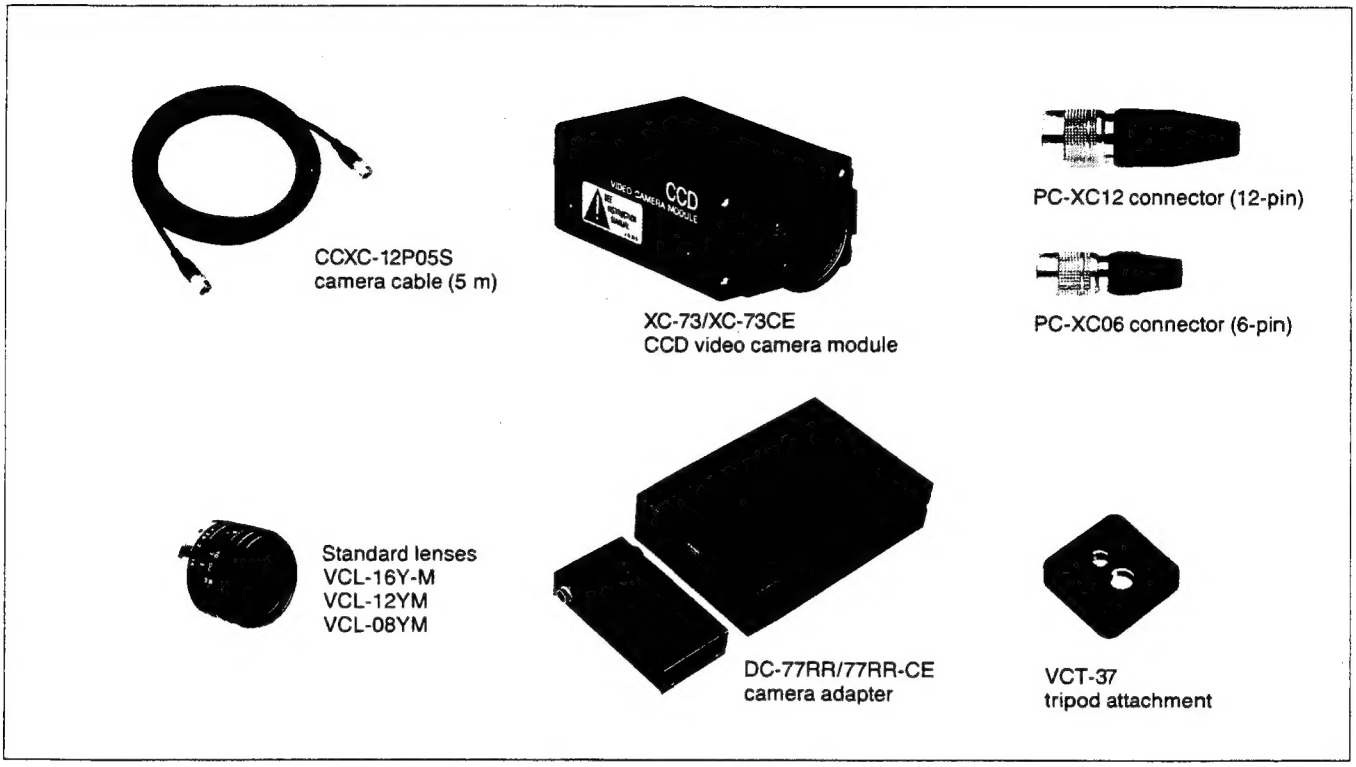
This camera module can directly replace a series XC-77 camera module, because the cross section size, the VIDEO OUT connector, and the pin assignments of the 12-pin connectors, are all common with those of the series XC-77.

### Other features

- Long life and high reliability
- Fine image, minimum distortion
- High resistance to vibration and impact
- Quick start-up
- Stability against even strong magnetic fields
- Low power consumption (1.4 W)

## 1-2. System Components

The CCD camera module XC-73/73CE system comprises the following optional products (available separately).




### XC-73/73CE video camera module

This is a small-size, high-resolution, monochrome video camera module using a 1/3 inches CCD image sensor.

### VCL-08YM standard lens

This is a standard f/1.4 lens of focal length 8 mm. The iris and focus are manually adjusted.

### CCXC-12P05S/05D/05R/05U camera cable (5 m)

This is attached to the DC IN/SYNC connector of the camera module with a 12-pin connector and is used for power supply, transmission of video signals, and exchange of sync signals.

### PC-XC12 connector (12-pin)

This is used to attach the camera cable to the DC IN/SYNC connector of the camera module.

### PC-XC06 connector (6-pin)

This is used to connect the lens cable of an auto-iris lens to the LENS connector of the camera module.

### DC-77RR/77RR-CE camera adapter

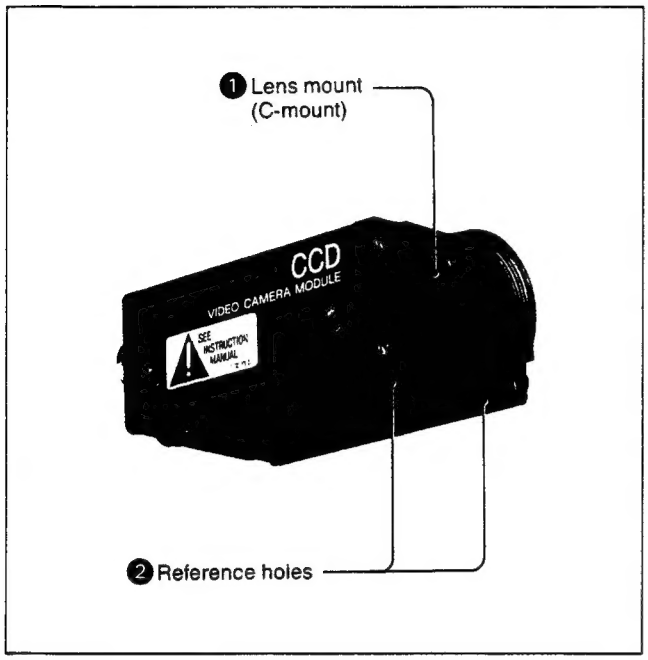
This is connected to the camera module to enable power supply from ordinary AC power source, and also handles transmission of video signals from the camera module and exchange of sync signals between the camera module and an external sync signal generator.

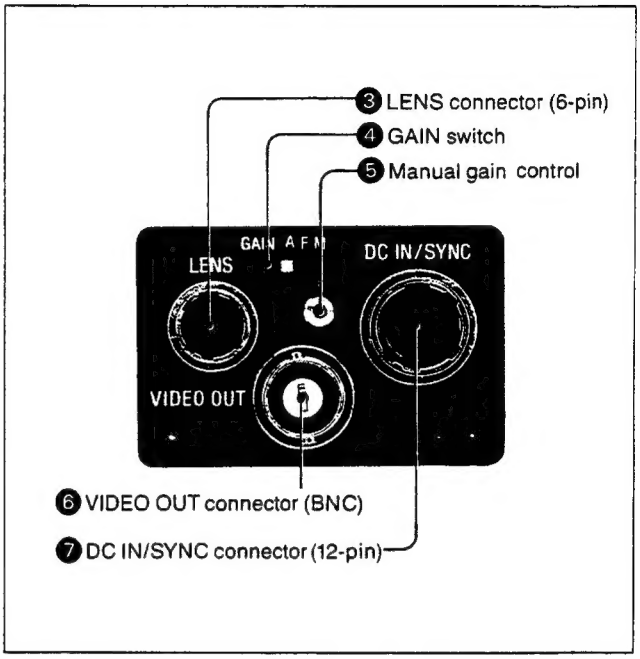
### VCT-37 tripod attachment

This attaches to the bottom of the camera module to fix the camera module to a tripod.

## 1-3. Location and Function of Parts and Operation

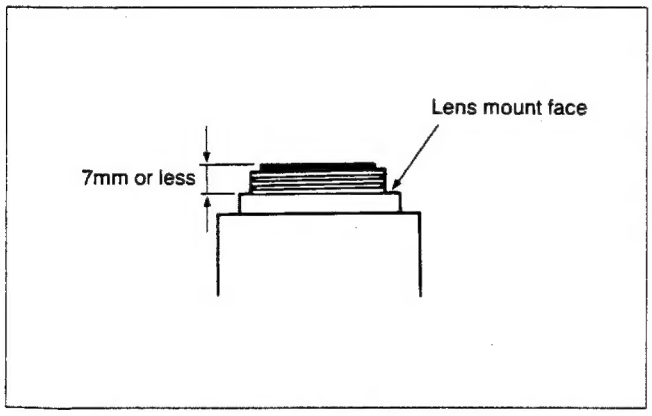
### XC-73/73CE CCD Video Camera Module




**❶ Lens mount**
Attach a VCL-08YM standard lens, or any C-mount lens or other optical equipment.

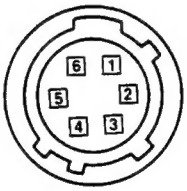
**Note**
The lens must not project more than 7 mm from the lens mount.




**❷ Reference holes**
These screw holes are precisely cut for camera module mounting. Using these holes assures accurate alignment of the optical axis.

*Refer to the service manual for detailed dimensions.*

**❸ LENS connector (6-pin)**
The lens cable of an auto-iris lens plugs into this connector, for automatic iris control.
The pin configuration of this connector is as follows.




| Pin No. | Signal |
|---|---|
| 1 | FLD signal output |
| 2 | Trigger |
| 3 | Ground |
| 4 | — |
| 5 | Video signal output |
| 6 | +12 V DC output |

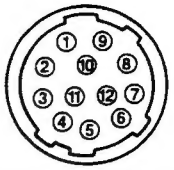
**❹ GAIN switch**
This switch selects AGC (A), fixed gain (F), or manual gain control (M).

**❺ Manual gain control**
In manual gain mode, this controls the gain level.

**❻ VIDEO OUT (Video signal output) connector (BNC)**
You can use this connector for video signal output from the camera module. The CCXC-12P05S camera cable must be attached to the DC IN/SYNC connector and the video signal output from the DC IN/SYNC connector must not have a 75-ohm termination.

### ⑦ DC IN/SYNC (DC power input/sync signal I/O) connector (12-pin)

Connect a CCXC-12P05S camera cable to this connector for the +12 V DC power supply and the video signal output from the camera module. When a sync signal generator is connected to this connector, the camera module is synchronized with the external sync signals. The pin configuration of this connector is as follows.



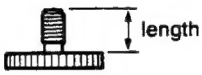

| Pin No. | External sync mode | | | Camera sync output |
|---|---|---|---|---|
| | HD, VD | VS | Restart/Reset | |
| 1 | Ground | Ground | Ground | Ground |
| 2 | +12 V DC | +12 V DC | +12 V DC | +12 V DC |
| 3 | Video output (Ground) | Video output (Ground) | Video output (Ground) | Video output (Ground) |
| 4 | Video output (Signal) | Video output (Signal) | Video output (Signal) | Video output (Signal) |
| 5 | HD input (Ground) | — | HD input (Ground) | HD onput (Ground) |
| 6 | HD input (signal) | — | HD input (signal) | HD output* (signal) |
| 7 | VD input (Signal) | VS input (Signal) | Reset (Signal) | VD output* (Signal) |
| 8 | — | — | — | Clock output (Ground) |
| 9 | — | — | — | Clock output** (Signal) |
| 10 | Ground | Ground | — | Ground |
| 11 | +12 V DC | +12 V DC | — | +12 V DC |
| 12 | VD input (Ground) | VD input (Ground) | Reset (Ground) | VD output (Ground) |

* An internal switch change is necessary to output HD, VD signals. See the service manual for details.

** An internal jumper change is necessary to output the clock signal. See the service manual for details.

## VCT-37 Tripod Attachment

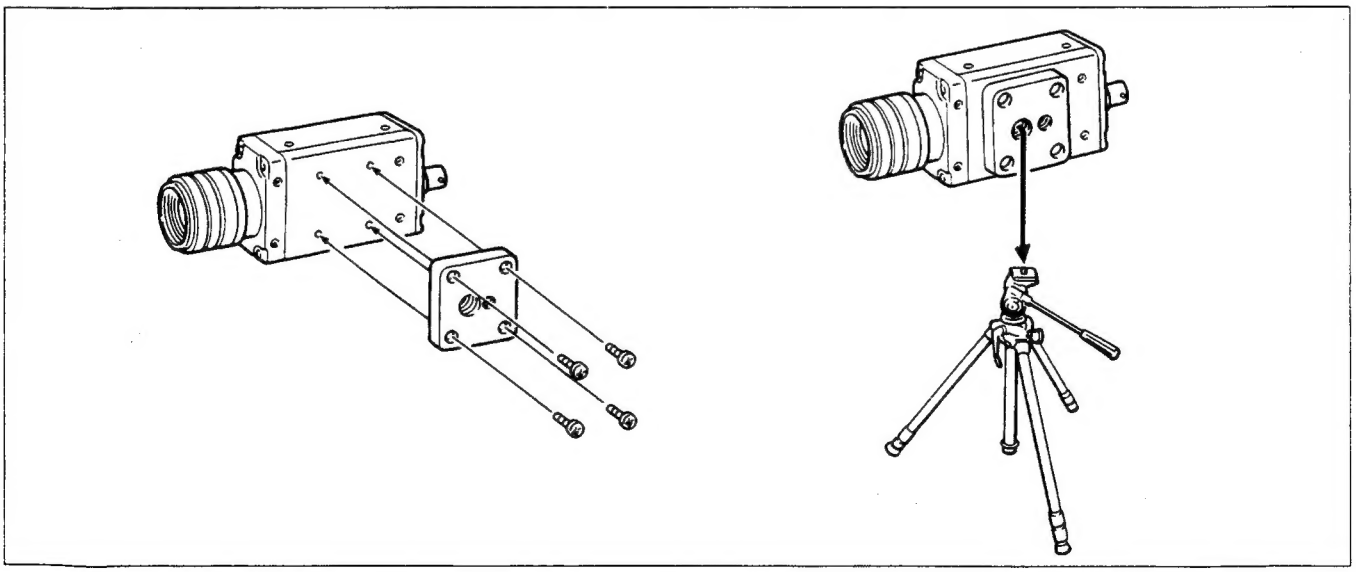
Use a tripod with screws meeting either of the following specifications.
ISO standard: length 4.5 mm ±0.2 mm
ASA standard: length 0.197 inches




**Note**

Use screws with a maximum length of 4 mm to fix the tripod attachment to the CCD video camera module.

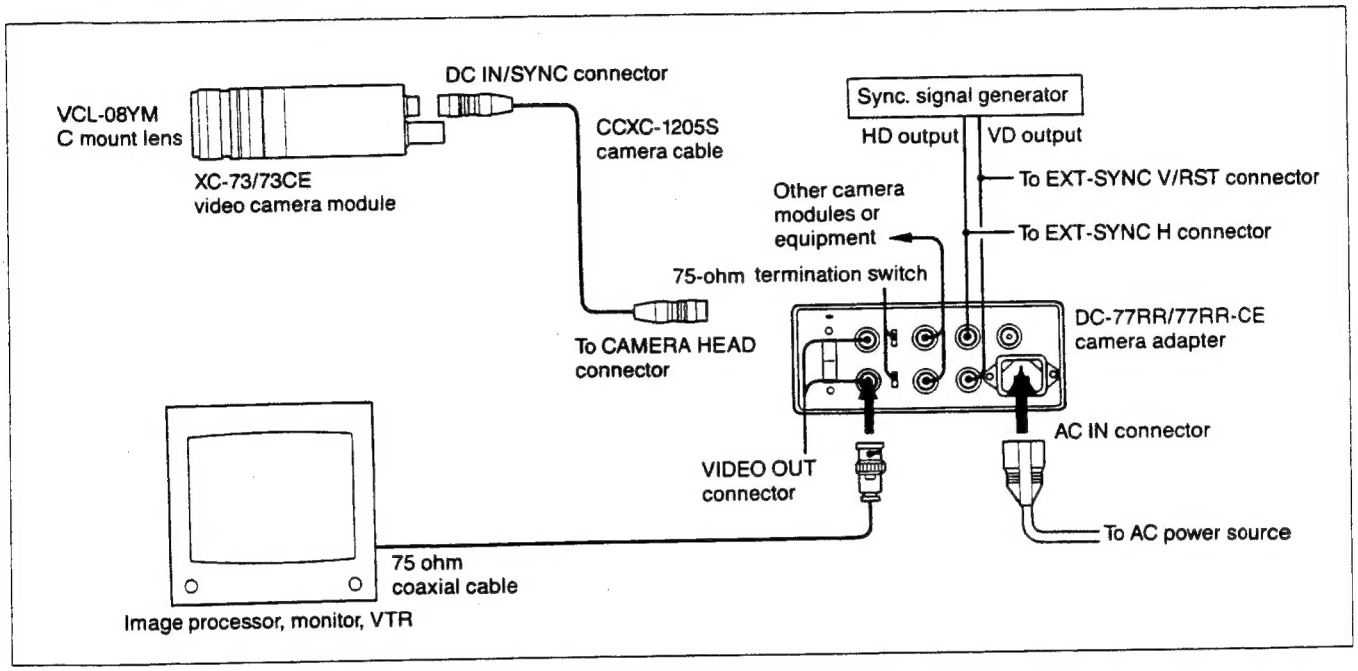
### Attaching the tripod attachment to the video camera module



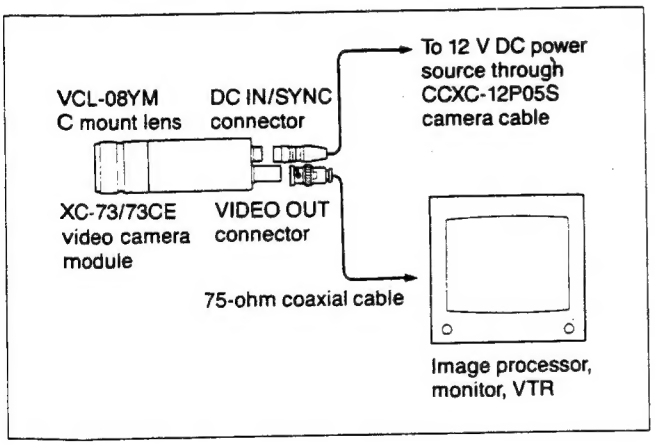
## 1-4. Connections

### Connection to AC power source

Connect the camera module to a DC-77RR/77RR-CE adapter for AC power supply. See the manual for the DC-77RR/77RR-CE for details.




### Direct connection to DC power source




**Note**

You can take the video output from the VIDEO OUT connector while supplying power through the DC IN/SYNC connector. Connect the camera module to the DC IN/SYNC connector with a CCXC-12P05S camera cable, and do not terminate the video signals from the DC IN/SYNC connector with 75 ohm.

## 1-5. Factory Settings

The following table lists the factory default settings for the various adjustments.
See the service manual and the operation manual for the DC-77RR/77RR-CE camera adapter for details.

| Item | Setting | Remarks |
|---|---|---|
| Gain | A<br>[F]<br>M | AGC<br>Fixed gain<br>Manual gain control |
| γ | ON<br>[OFF] | Compensated<br>Not compensated |
| 75-ohm termination | [ON]<br>OFF | Terminated<br>Not terminated |
| HD/VD signals | [EXT IN]<br>INT OUT | External signal input<br>Internal signal output |
| Electronic shutter | [OFF]<br>FL<br>1/125, 1/250, 1/500, 1/1000, 1/2000, 1/10000 (sec) | Flickerless |
| Restart/ Reset | ON<br>[OFF] | Frame sync<br>Not frame sync |
| Charge accumulation | [FRAME]<br>FIELD | Frame accumulation<br>Field accumulation |

## 1-6. Notes on Operation

### Power supply

The camera operates on 12 V DC. Use a stable power source free from ripple or noise.

### Foreign bodies

Be careful not to spill liquids, or drop any flammable or metal objects in the camera body.

### Heat radiation

Do not wrap the camera in cloth or other material while in operation. There is a danger of overheating.

### Locations for operation and storage

Avoid operation or storage in the following places.
- Extremely hot or cold locations. Recommended temperature range is 0°C to 40°C. (32°F to 104°F)
- Humid or dusty locations
- Locations exposed to rain
- Locations subject to strong vibration
- Near generators of strong electromagnetic radiation such as TV or radio transmitters.

### Care

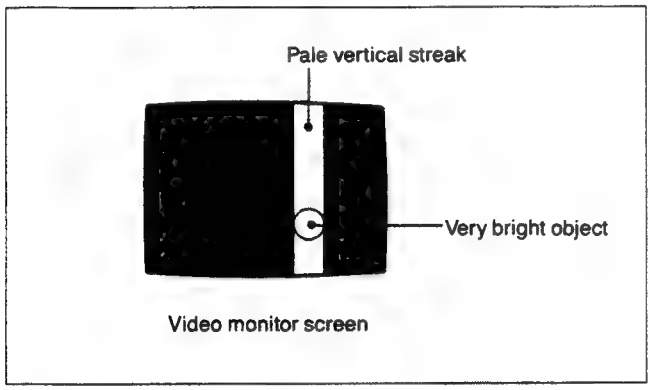
Use a blower to remove dust from the surface of the lens or optical filter. Clean the exterior with a soft, dry cloth. If the camera is very grimy, apply a cloth soaked in a mild detergent then wipe with a dry cloth. Do not apply organic solvents such as alcohol which may damage the finish.

## 1-7. Typical CCD Phenomena

The following effects on the monitor screen are characteristic of CCD cameras. They do not indicate any fault with the camera module.

### Smear

This occurs when you shoot a very bright object such as electric lighting, the sun, or a strong reflection (shown below).




This phenomenon is caused by an electric charge induced by infrrared radiation deep in the photosensor. It appears as a vertical smear because the CCD imaging element uses the interline transfer system.

### Vertical aliasing

When you shoot vertical stripes or lines, they may appear jagged.

### Blemishes

A CCD image sensor consists of an array of individual sensor elements (pixels). A malfunctioning sensor element will cause a single pixel blemish in the picture. (This is not a problem in practice).

### White speckle

When you shoot a dark object at high temperature, small white dots may appear all over the image.

# SECTION 1
# OPERATION

## 1-1. Overview

The XC-75/75CE is a monochrome video camera module using a CCD (Charge Coupled Device) solid state image sensor.

### High image quality

The CCD provides a high-resolution image with 768 × 494 pixels (XC-75) or 752 × 582 pixels (XC-75CE).

### Range of operating modes

You can easily select the required operating mode. The gain, for example, can be set to AGC (A), or to fixed gain (F) or manual gain control (M) by an external switch.
* $\gamma$ (gamma) compensation can be switched on or off by an internal jumpers.By an internal jumper connection to switch the charge accumulation mode from frame to field, if external sync signals in noninterlace mode are input, the same sensitivity can be obtained as in interlace mode.

* The internal switch is mounted instead of internal jumpers in the following serial number for the camera module.
Serial number ;
XC-75 (UCJ) : 10001 - 60900
XC-75CE (EK) : 10001 - 53000

### External synchronization

The camera module can be synchronized with three types of signals explained below. The capture frequency range is ±1% of the horizontal scan frequency.
HD (horizontal drive), VD (vertical drive) signals: The camera module automatically determines whether to operate in interlace or noninterlace mode from the HD and VD signals input for external synchronization.
VS (Video/Sync) signals: External synchronization with a video or composite sync signal. (The unit switches automatically between HD/VD and VS synchronization.)
Reset pulse signal: The timing for reading out the contents of the register can be adjusted by the reset pulse signal.

### Internal sync signal output

FLD (Field Index) signals are output constantly from the 6-pin connector. An internal switch change allows the HD and VD signals also to be output from the 12-pin connectors.

### Electronic shutter function

Shutter speed can be selected from a wide range (1/125 to 1/10000 sec.) or in flickerless (FL) mode.

### Body fixing

Two mounting screw holes are provided in the reference plane on the lower surface of the body, allowing mounting with the absolute minimum deviation of the optical axis.

### Compatibility with the series XC-77

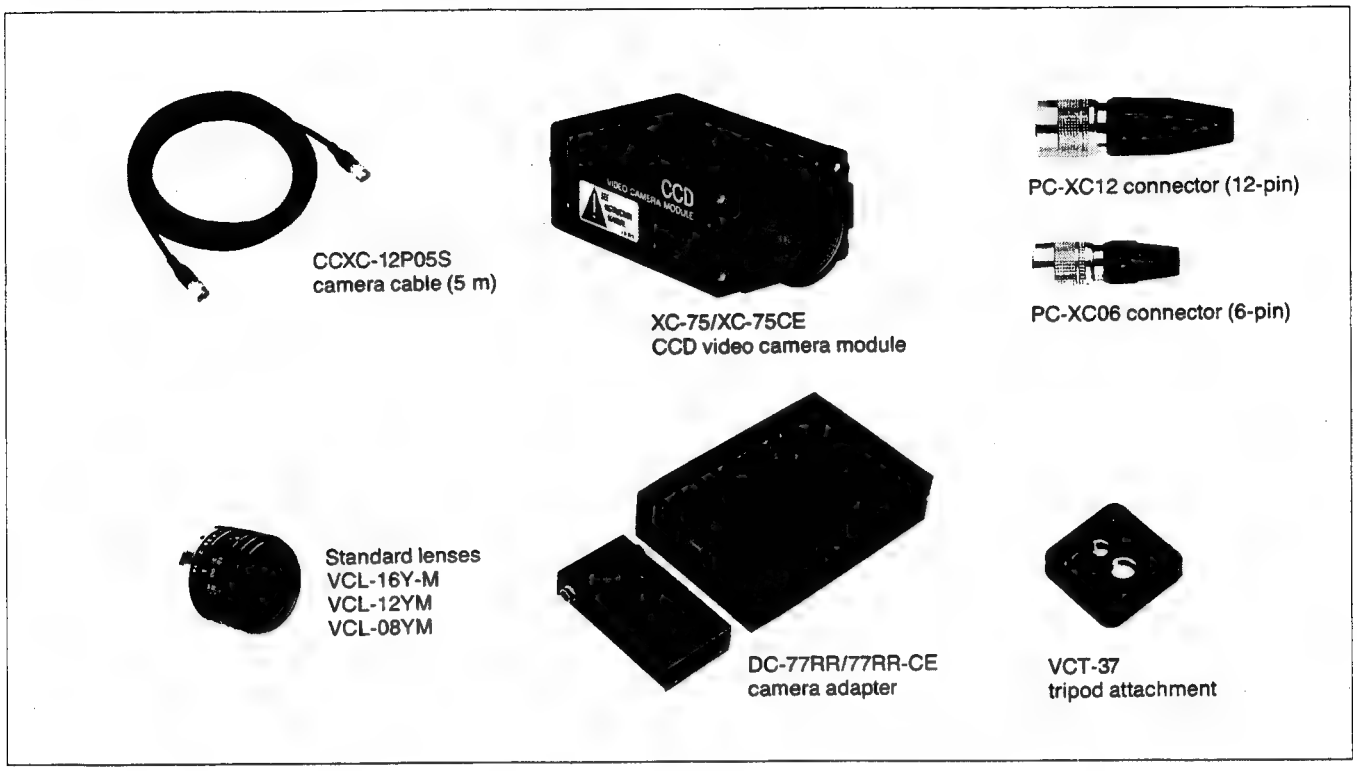
This camera module can directly replace a series XC-77 camera module, because the cross section size, the VIDEO OUT connector, and the pin assignments of the 12-pin connectors, are all common with those of the series XC-77.

### Other features

- Long life and high reliability
- Fine image, minimum distortion
- High resistance to vibration and impact
- Quick start-up
- Stability against even strong magnetic fields
- Low power consumption (1.6 W)

## 1-2. System Components

The CCD camera module XC-75/75CE system comprises the following optional products (available separately).




### XC-75/75CE video camera module

This is a small-size, high-resolution, monochrome video camera module using a 1/2 inches CCD image sensor.

### VCL-12YM standard lens

This is a standard f/1.8 lens of focal length 12 mm. The iris and focus are manually adjusted.

### CCXC-12P05S/05D/05R/05U camera cable (5 m)

This is attached to the DC IN/SYNC connector of the camera module with a 12-pin connector and is used for power supply, transmission of video signals, and exchange of sync signals.

### PC-XC12 connector (12-pin)

This is used to attach the camera cable to the DC IN/SYNC connector of the camera module.

### PC-XC06 connector (6-pin)

This is used to connect the lens cable of an auto-iris lens to the LENS connector of the camera module.

### DC-77RR/77RR-CE camera adapter

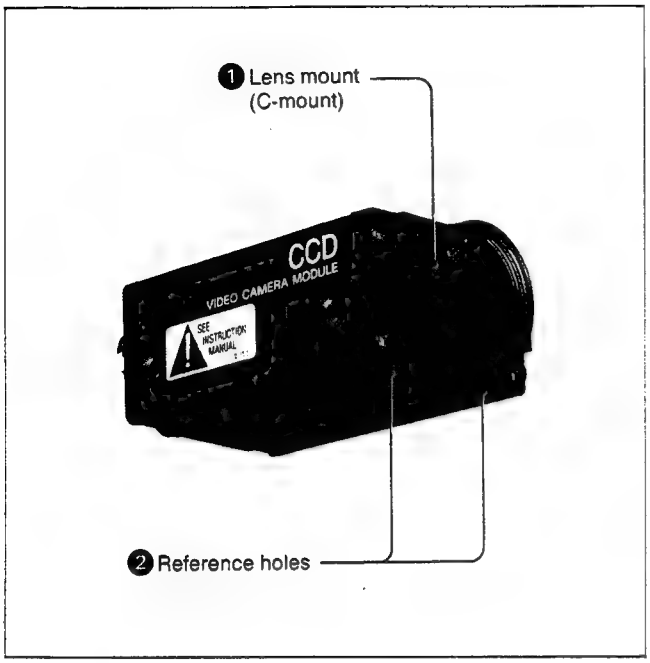
This is connected to the camera module to enable power supply from ordinary AC power source, and also handles transmission of video signals from the camera module and exchange of sync signals between the camera module and an external sync signal generator.

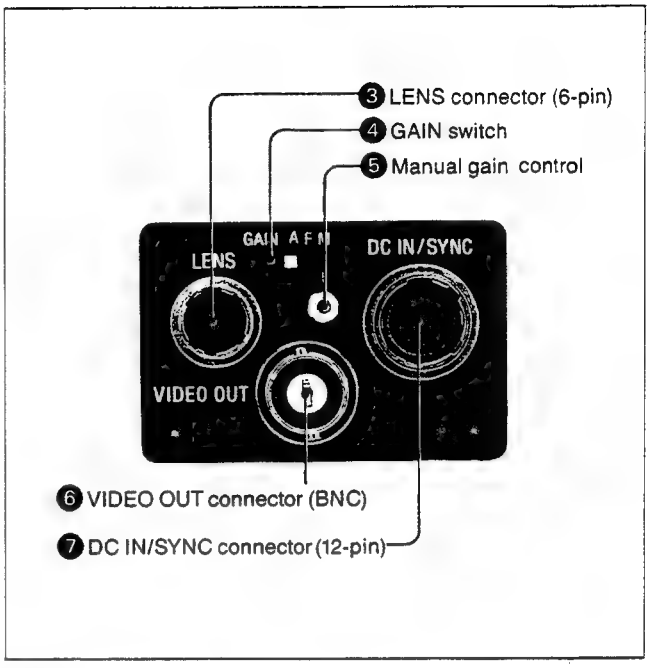
### VCT-37 tripod attachment

This attaches to the bottom of the camera module to fix the camera module to a tripod.

## 1-3. Location and Function of Parts and Operation

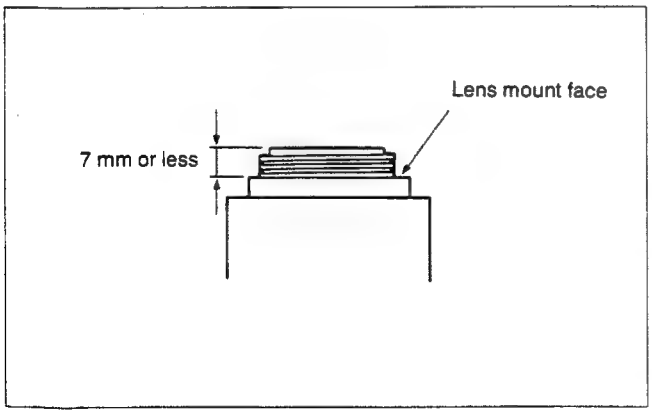
### XC-75/75CE CCD Video Camera Module




**1 Lens mount**
Attach a VCL-12YM standard lens, or any C-mount lens or other optical equipment.

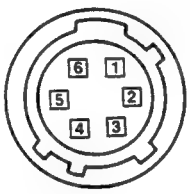
**Note**
The lens must not project more than 7 mm from the lens mount.




**2 Reference holes**
These screw holes are precisely cut for camera module mounting. Using these holes assures accurate alignment of the optical axis.

*Refer to the service manual for detailed dimensions.*

**3 LENS connector (6-pin)**
The lens cable of an auto-iris lens plugs into this connector, for automatic iris control.
The pin configuration of this connector is as follows.




| Pin No. | Signal |
|---|---|
| 1 | FLD signal output |
| 2 | Trigger |
| 3 | Ground |
| 4 | — |
| 5 | Video signal output |
| 6 | +12 V DC output |

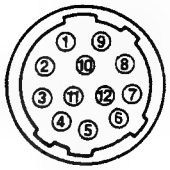
**4 GAIN switch**
This switch selects AGC (A), fixed gain (F), or manual gain control (M).

**5 Manual gain control**
In manual gain mode, this controls the gain level.

**6 VIDEO OUT (Video signal output) connector (BNC)**
You can use this connector for video signal output from the camera module. The CCXC-05S camera cable must be attached to the DC IN/SYNC connector and the video signal output from the DC IN/SYNC connector must not have a 75-ohm termination.

### ❼ DC IN/SYNC (DC power input/sync signal I/O) connector (12-pin)

Connect a CCXC-12P05S camera cable to this connector for the + 12V DC power supply and the video signal output from the camera module. When a sync signal generator is connected to this connector, the camera module is synchronized with the external sync signals. The pin configuration of this connector is as follows.




| Pin No. | External sync mode | | | Camera sync output |
|---|---|---|---|---|
| | HD, VD | VS | Restart/Reset | |
| 1 | Ground | Ground | Ground | Ground |
| 2 | + 12 V DC | + 12 V DC | + 12 V DC | + 12 V DC |
| 3 | Video output (Ground) | Video output (Ground) | Video output (Ground) | Video output (Ground) |
| 4 | Video output (Signal) | Video output (Signal) | Video output (Signal) | Video output (Signal) |
| 5 | HD input (Ground) | — | HD input (Ground) | HD onput (Ground) |
| 6 | HD input (signal) | — | HD input (signal) | HD output* (signal) |
| 7 | VD input (Signal) | VS input (Signal) | Reset (Signal) | VD output* (Signal) |
| 8 | — | — | — | Clock output (Ground) |
| 9 | — | — | — | Clock output** (Signal) |
| 10 | Ground | Ground | — | Ground |
| 11 | + 12 V DC | + 12 V DC | — | + 12 V DC |
| 12 | VD input (Ground) | VD input (Ground) | Reset (Ground) | VD output (Ground) |

* An internal switch change is necessary to output HD, VD signals. See the service manual for details.

** An internal jumper change is necessary to output the clock signal. See the service manual for details.

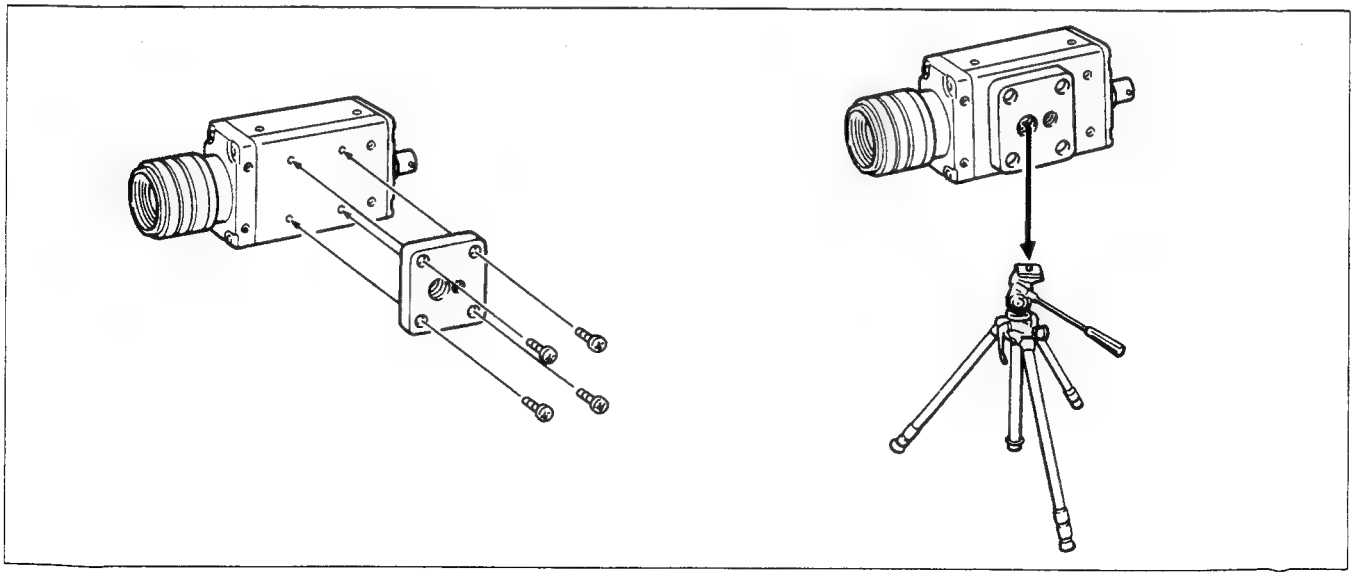
## VCT-37 Tripod Attachment

Use a tripod with screws meeting either of the following specifications.
ISO standard: length 4.5 mm ±0.2 mm
ASA standard: length 0.197 inches


**Note**

Use screws with a maximum length of 4 mm to fix the tripod attachment to the CCD video camera module.

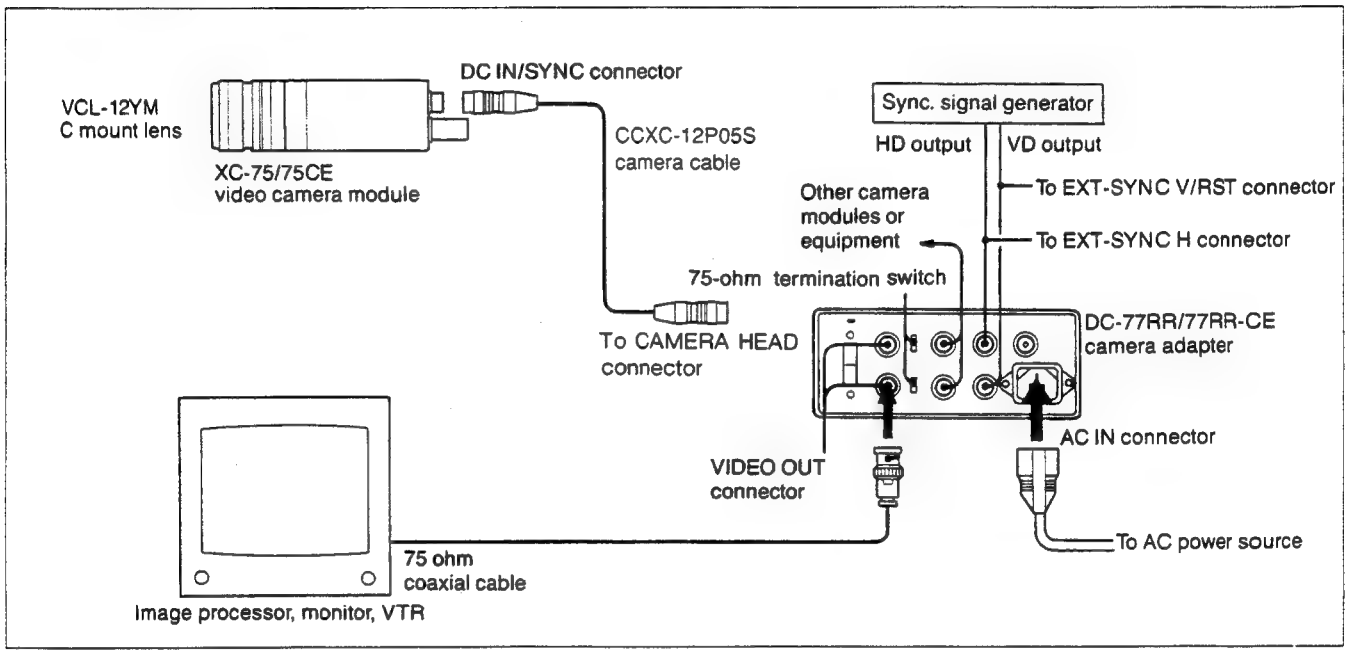
### Attaching the tripod attachment to the video camera module



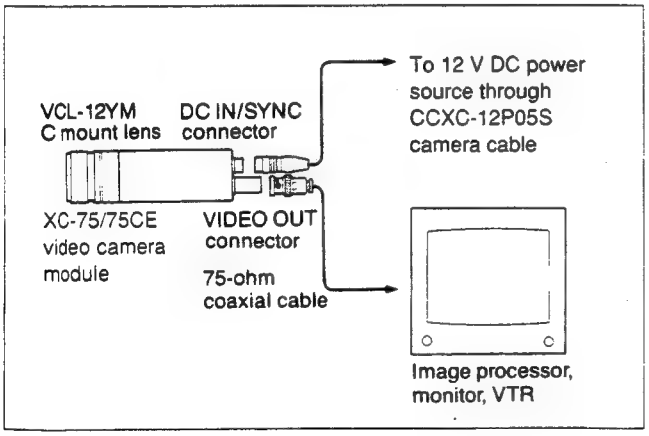
## 1-4. Connections

### Connection to AC power source

Connect the camera module to a DC-77RR/77RR-CE adapter for AC power supply. See the manual for the DC-77RR/77RR-CE for details.




### Direct connection to DC power source




**Note**

You can take the video output from the VIDEO OUT connector while supplying power through the DC IN/SYNC connector. Connect the camera module to the DC IN/SYNC connector with a CCXC-12P05S camera cable, and do not terminate the video signals from the DC IN/SYNC connector with 75 ohm.

## 1-5. Factory Settings

The following table lists the factory default settings for the various adjustments.
See the service manual and the operation manual for the DC-77RR/77RR-CE camera adapter for details.

| Item | Setting | Remarks |
|---|---|---|
| Gain | A<br>[F]<br>M | AGC<br>Fixed gain<br>Manual gain control |
| γ | ON<br>[OFF] | Compensated<br>Not compensated |
| 75-ohm termination | [ON]<br>OFF | Terminated<br>Not terminated |
| HD/VD signals | [EXT IN]<br>INT OUT | External signal input<br>Internal signal output |
| Electronic shutter | [OFF]<br>FL<br>1/125, 1/250, 1/500, 1/1000, 1/2000, 1/10000 (sec) | Flickerless |
| Restart/ Reset | ON<br>[OFF] | Frame sync<br>Not frame sync |
| Charge accumulation | [FRAME]<br>FIELD | Frame accumulation<br>Field accumulation |

## 1-6. Notes on Operation

### Power supply

The camera operates on 12 V DC. Use a stable power source free from ripple or noise.

### Foreign bodies

Be careful not to spill liquids, or drop any flammable or metal objects in the camera body.

### Heat radiation

Do not wrap the camera in cloth or other material while in operation. There is a danger of overheating.

### Locations for operation and storage

Avoid operation or storage in the following places.
- Extremely hot or cold locations. Recommended temperature range is 0°C to 40°C. (32°F to 104°F)
- Humid or dusty locations
- Locations exposed to rain
- Locations subject to strong vibration
- Near generators of strong electromagnetic radiation such as TV or radio transmitters.

### Care

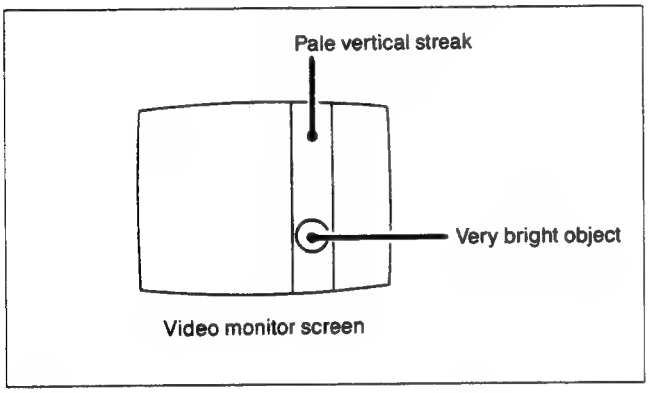
Use a blower to remove dust from the surface of the lens or optical filter. Clean the exterior with a soft, dry cloth. If the camera is very grimy, apply a cloth soaked in a mild detergent then wipe with a dry cloth. Do not apply organic solvents such as alcohol which may damage the finish.

## 1-7. Typical CCD phenomena

The following effects on the monitor screen are characteristic of CCD cameras. They do not indicate any fault with the camera module.

### Smear

This occurs when you shoot a very bright object such as electric lighting, the sun, or a strong reflection (shown below).




This phenomenon is caused by an electric charge induced by infrrared radiation deep in the photosensor. It appears as a vertical smear because the CCD imaging element uses the interline transfer system.

### Vertical aliasing

When you shoot vertical stripes or lines, they may appear jagged.

### Blemishes

A CCD image sensor consists of an array of individual sensor elements (pixels). A malfunctioning sensor element will cause a single pixel blemish in the picture. (This is not a problem in practice).

### White speckle

When you shoot a dark object at high temperature, small white dots may appear all over the image.

# SECTION 2
# COMPREHENSIVE SPECIFICATIONS

## 2-1. SPECIFICATIONS(XC-73/75)

### Imaging system

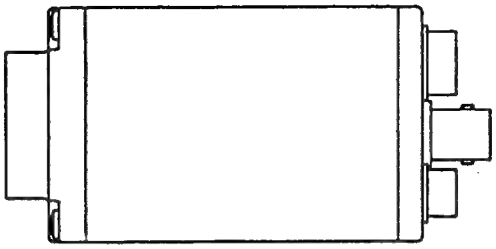
| | | |
|---|---|---|
| Pickup device | Interline-transfer CCD | |
| Effective picture elements | | |
| | XC-75: | 768 × 494 (horizontal/vertical |
| Sensing area | XC-73: | 1/3-inch size |
| | XC-75: | 1/2-inch size |
| Optical blank | 43 elements on each horizontal line. | |
| CCD vertical drive frequency | 15.734 kHz ± 1% | |
| CCD horizontal drive frequency | 14.318 MHz | |
| Signal system | EIA system | |
| Cell size | XC-73: | 6.35 × 7.4 μ m (horizontal/vertical) |
| | XC-75: | 8.4 × 9.8 μ m (horizontal/vertical) |

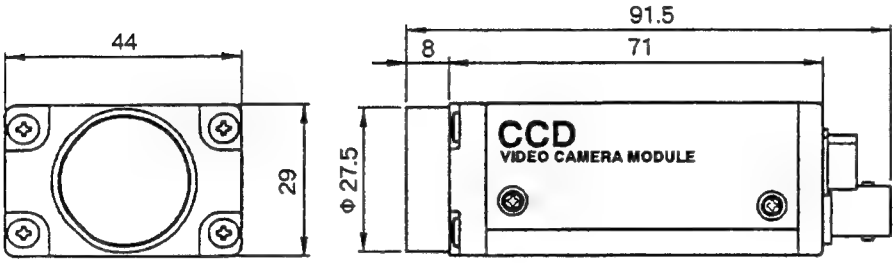
### Optical system and others

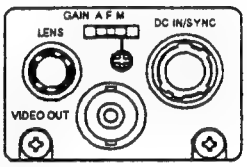
| | |
|---|---|
| Lens mount | C mount |
| Flunge focal length | 17.526 mm |
| Synchronization | Internal/external (automatically switched according to input signal) |
| External sync signal | S, VS (sync level: $0.3^{+0.3}_{-0.15}$ Vp-p) |
| I/O | HD/VD (HD/VD level: 2-5 Vp-p, automatically switched between HD/VD according to input signal, and I/O selection by internal switch) |
| External sync allowable frequency | ± 1% (of horizontal sync frequency) |
| Jitter | Within ± 50 nsec |
| Scanning system | 525 lines 2:1 interlace/noninterlace (automatically switched according to input signal) |
| Video output | 1.0 Vp-p, sync negative, 75 ohms unbalanced |
| Horizontal resolution (When using VCL-08 YM lens with any iris adjustment from "open" to F11) | 570 TV lines |
| Vertical effective lines | 485 lines (with 2:1 interlace) |
| Sensitivity | 400 lux, F4 ( γ compensation ON, 0 dB) |
| Minimum illumination | 3.0 lux (AGC mode, F1.4, γ compensation ON) |
| Video S/N ratio | 56 dB |
| Gain | AGC/Fixed gain/Manual gain control (selected by switch on the rear panel) |
| γ | γ compensation/ γ =1 * (selected by internal jumpers) * The internal switch is mounted instead of internal jumpers in the following serial number for the camera module. Serial number ; XC-73 (UCJ) : 10001 - 15550 XC-75 (UCJ) : 10001 - 60900 |
| White clip | 115 IRE ± 10 IRE |
| Charge accumulation | Frame/Field (switched by internal jumper change) |
| Shutter | Normal shutter/Special shutter (switched by internal jumper change) |
| Shutter speed | Normal shutter: Flickerless 1/125, 1/250, 1/500, 1/1000, 1/2000, 1/10000 sec. (selected by internal switch) Special shutter: 1/1600 to 1/100 sec. |
| Power | +12 V DC (Range: 10.5 to 15 V) |
| Power consumption | XC-73: 1.4 W XC-75: 1.6 W |
| Temperature | Operating: -5 to +45 °C (41 to 113 °F) Storage: -25 to +60 °C ) (77 to 140 °F) |
| Relative humidity | Operating: 20 to 80 % Storage: 20 to 95 % |
| Vibration resistance | 7 G (11 Hz-200 Hz) |
| Shock resistance | 70 G |
| External dimension (w/h/d) | 44 × 29 × 91.5 mm (1 3/4 × 1 3/6 × 3 5/8 inches) (including external projection) |
| Mass | 140 g (5 oz) |
| Accessories | Lens mount cap (1) Operation manual (1) |

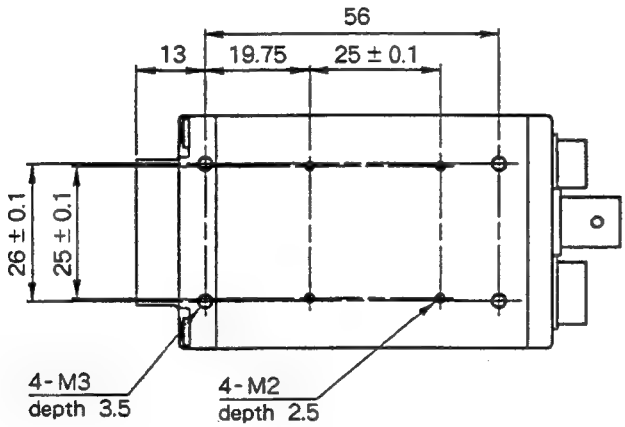
Design and specifications are subject to change without notice.

**Dimensions:**
**Camera Module <XC-75>**

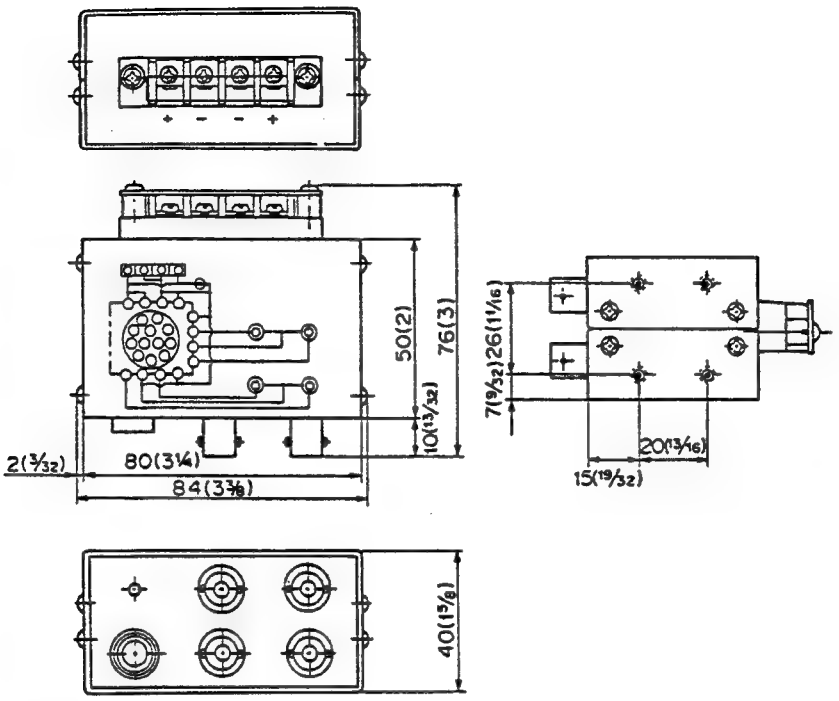




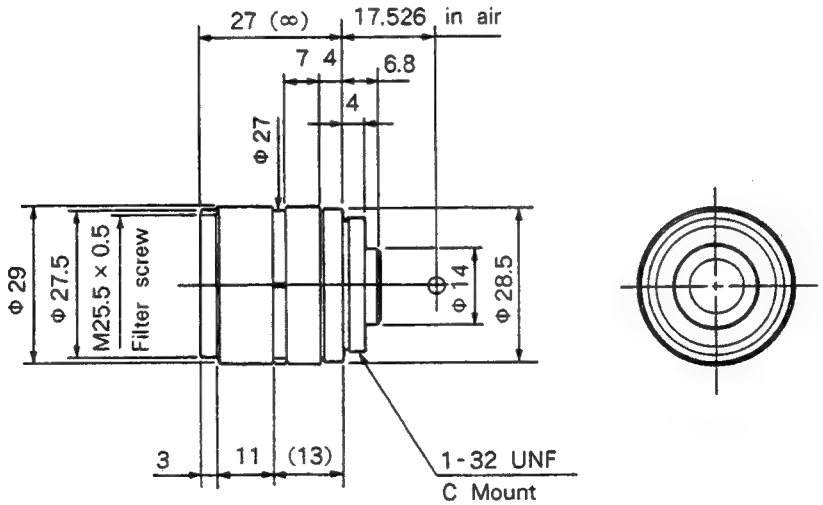



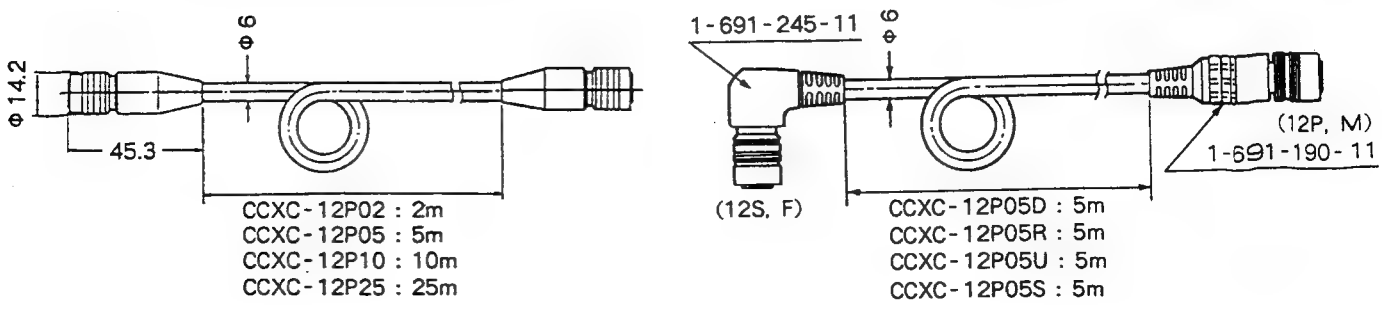
**Junction box**




**Lens**

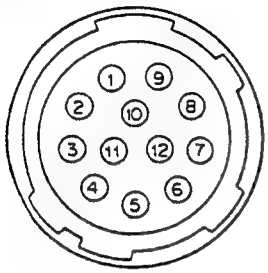



**Camera cable**



## 2-2. CONNECTORS PIN FUNCTION

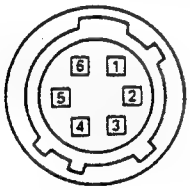
### 12P Multiconnector (External view)




| PIN No. | EXTERNAL SYNC MODE | | | CAMERA SYNCRONOUS OUTPUT |
|---|---|---|---|---|
| | HD/VD | VS | RESTART RESET | |
| 1 | GND | GND | GND | GND |
| 2 | DC+12V | DC+12V | DC+12V | DC+12V |
| 3 | VIDEO OUTPUT (GND) | VIDEO OUTPUT (GND) | VIDEO OUTPUT (GND) | VIDEO OUTPUT (GND) |
| 4 | VIDEO OUTPUT (SIGNAL) | VIDEO OUTPUT (SIGNAL) | VIDEO OUTPUT (SIGNAL) | VIDEO OUTPUT (SIGNAL) |
| 5 | HD INPUT (GND) | — | HD INPUT (GND) | HD OUTPUT (GND) |
| 6 | HD INPUT (SIGNAL) | — | HD INPUT (SIGNAL) | HD OUTPUT (SIGNAL) |
| 7 | VD INPUT (SIGNAL) | VS INPUT (SIGNAL) | RESET PULSE (SIGNAL) | VD OUTPUT (SIGNAL) |
| 8 | — | — | — | CLOCK OUTPUT (GND) |
| 9 | — | — | — | CLOCK OUTPUT (SIGNAL) |
| 10 | GND | GND | GND | GND |
| 11 | DC+12V | DC+12V | DC+12V | DC+12V |
| 12 | VD INPUT (GND) | VS INPUT (GND) | RESET PULSE (GND) | VD OUTPUT (GND) |

NOTE HD/VD input level ; 2-5Vp-p, negative *
VS SYNC level ; 0.3-1.2Vp-p, negative *
* Either 75- Ω termination input or high impedance input is selectable using S2/SG-199 board.

### 6P Lens Connector (External view)

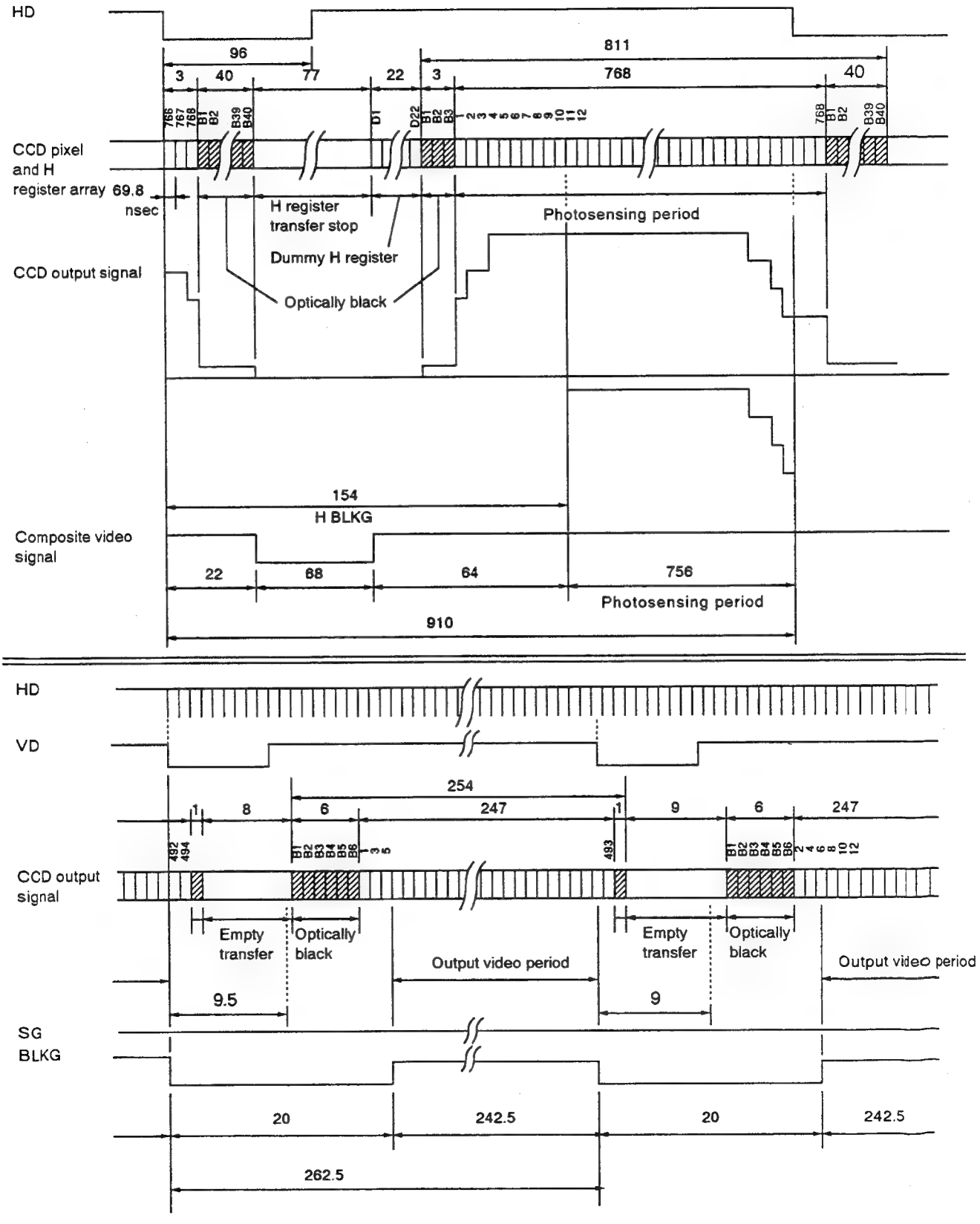



| PIN No. | SIGNAL | SPECIFICATION |
|---|---|---|
| 1 | FLD OUT | FLD IN |
| 2 | TRIGGER | TRRIGER |
| 3 | GND | GND |
| 4 | NC | NC |
| 5 | VS OUT | VIDEO SIGNAL OUTPUT |
| 6 | +12 OUT | DC+12V OUT |

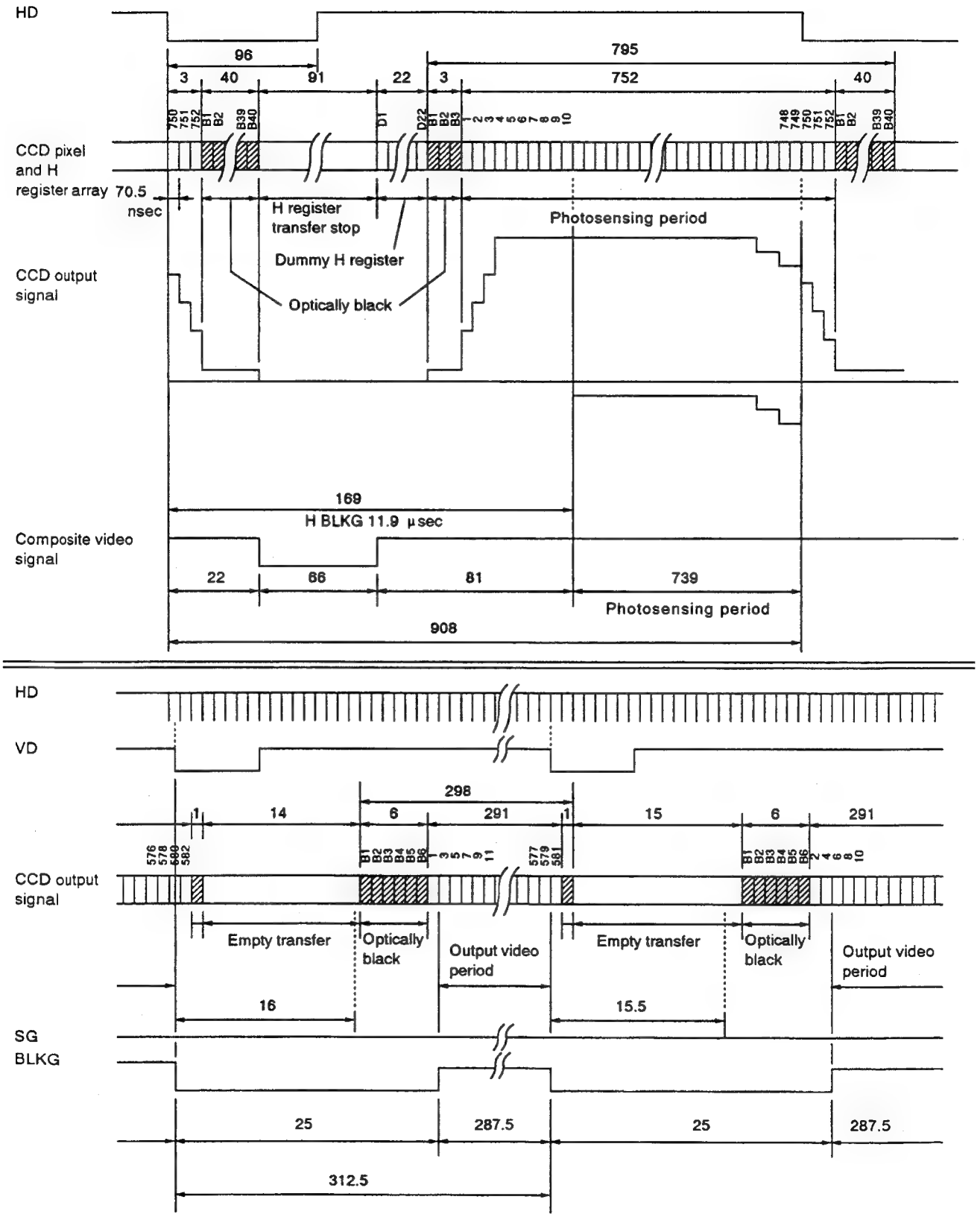
Note)
The video signal at pin ⑤ is for the AUTO-IRIS lens, so it cannot be terminated by 75 Ω.

## 2-3. TIMING CHART OF CCD OUTPUT WAVEFORMS

### 2-3-1. EIA



## 2-3-2. CCIR


HD
96
795
3
40
91
22
3
752
40
750
751
752
B1
B2
B39
B40
D1
D22
B1
B2
B3
1
2
3
4
5
6
7
8
9
10
748
749
750
751
752
B1
B2
B39
B40
CCD pixel and H register array
70.5 nsec
H register transfer stop
Dummy H register
Optically black
Photosensing period
CCD output signal
169
H BLKG 11.9 µsec
Composite video signal
22
66
81
739
Photosensing period
908
HD
VD
298
1
14
6
291
1
15
6
291
576
578
580
582
B1
B2
B3
B4
B5
B6
1
3
5
7
9
11
577
579
581
B1
B2
B3
B4
B5
B6
2
4
6
8
10
CCD output signal
Empty transfer
Optically black
Output video period
Empty transfer
Optically black
Output video period
16
15.5
SG
BLKG
25
287.5
25
287.5
312.5

## 2-4. EXTERNAL SYNCHRONIZATION

There are three external synchronization modes:
1. VS/VBS mode
2. HD and VD mode
3. RESTART RESET mode

### 2-4-1. VS/VBS Mode

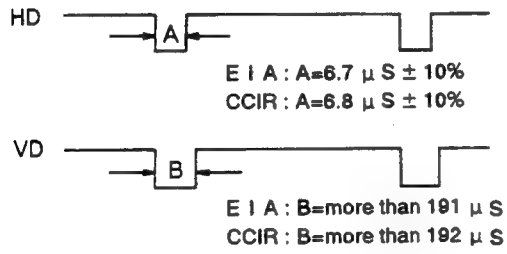
The VS/VBS mode provides external synchronization by supplying a normal composite signal, VS or VBS, to pin 7 of the 12-pin connector.

### 2-4-2. HD and VD Mode

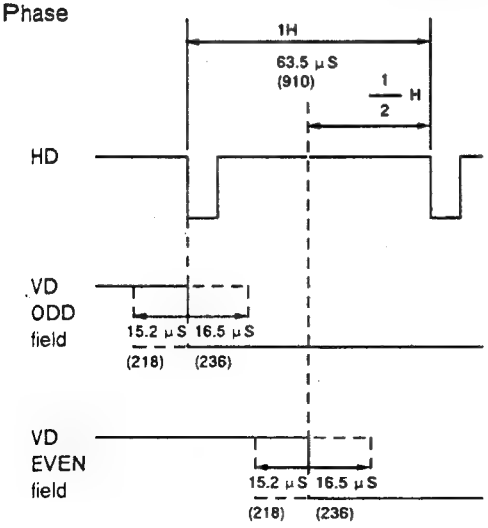
The HD and VD mode provides external synchronization by supplying an HD signal to pin 6 and a VD signal to pin 7 of the 12-pin connector.

**Input conditions of HD and VD signals**

- Frequency (period)
  HD : 15.734 kHz ± 1%(63.56 μs ± 1%)
  VD : 244 to 1023 1/2 H
  *The maximum number of vertical effective lines is 486 in the interlace mode.
  In the non-interlace mode, it is 242 for both the ODD field and the EVEN field.




- Phase




The figure in parentheses ( ) indicates the number of clock pulses

As shown in the illustration above, the ODD field is provided when the phase shift between the trailing edge of the VD signal and the trailing edge of the HD signal is between a lead of 15.2 μs and a lag of 16.5 μs. The EVEN field is provided when the phase shift between the trailing edge of the VD signal and the point 1/2H from the trailing edge of the HD signal is between a lead of 15.2 μs and a lag of 16.5 μs.

**Interlace and non-interlace**

Operation can be preformed in either interlace or non-interlace mode by changing the input condition of the VD signal. See Figure 1.

- Interlace
  To operate in the interlace mode, set the period of the VD signal to (A + 1/2)H. A is an integer, 244 to 1023. In other words, the phase of the leading edge of the VD signal against the leading edge of the HD signals is changed for each VD signal. The field changes from ODD to EVEN and to ODD, repeatedly during operation in the interlace mode. At this time, the number of scanning lines per frames is 2A + 1.

- Non-interlace
  To operate in the non-interlace mode, set the period of the VD signal to A H. A is an integer, 244 to 1023. In other words, the phase of the leading edge of the VD signal against the leading edge of the HD signal is not changed for each VD signal, and the field ODD or EVEN remains unchanged for operation in the non-interlace mode. The number of scanning lines is A; this is half of the number of scanning lines for operation in the interlace mode. The sensitivity is half of the sensitivity provided in the interlace mode, when the frame is stored. See Figure 2.

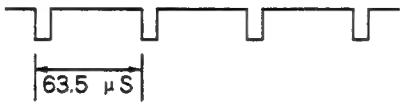
### 2-4-3. RESTART RESET Mode

In the RESTART RESET (R.R) mode, information for one screen can be retrieved at any time. It is necessary to internally set the R.R mode in the camera to provide the R.R mode. See Section 2 - 5. "OPERATION MODE SETTING".
Supply the HD and R.R signals to pin 6 and pin 7 of the 12-pin connector to obtain output.

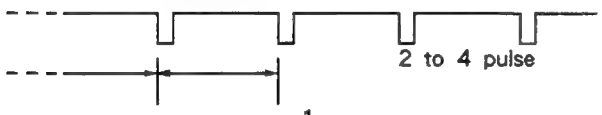
**Input conditions for the HD and R.R signals**

- Frequency(period)

HD signal : 15.734 kHz ± 1% (63.56 μs ± 1%)
Continuous pulse

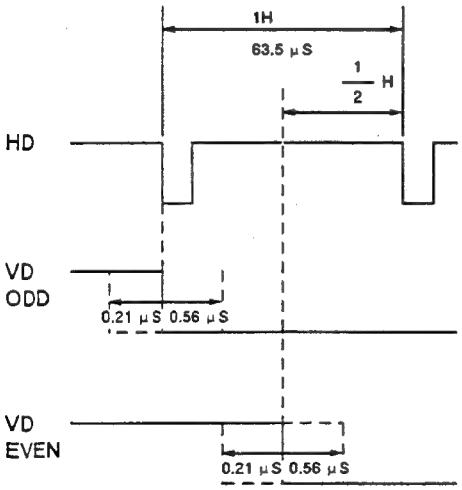



VD signal : 244 to 1023 1/2 H
2 to 4 pulses depending on the mode




Any time interval $244 \sim 1023\frac{1}{2}$ H

- Phase




- For the phase relation between external input HD and VD pulses, the allowance for the center phase in the specification is +8 clocks and - 3 clocks (maximum) as shown in the figure above.

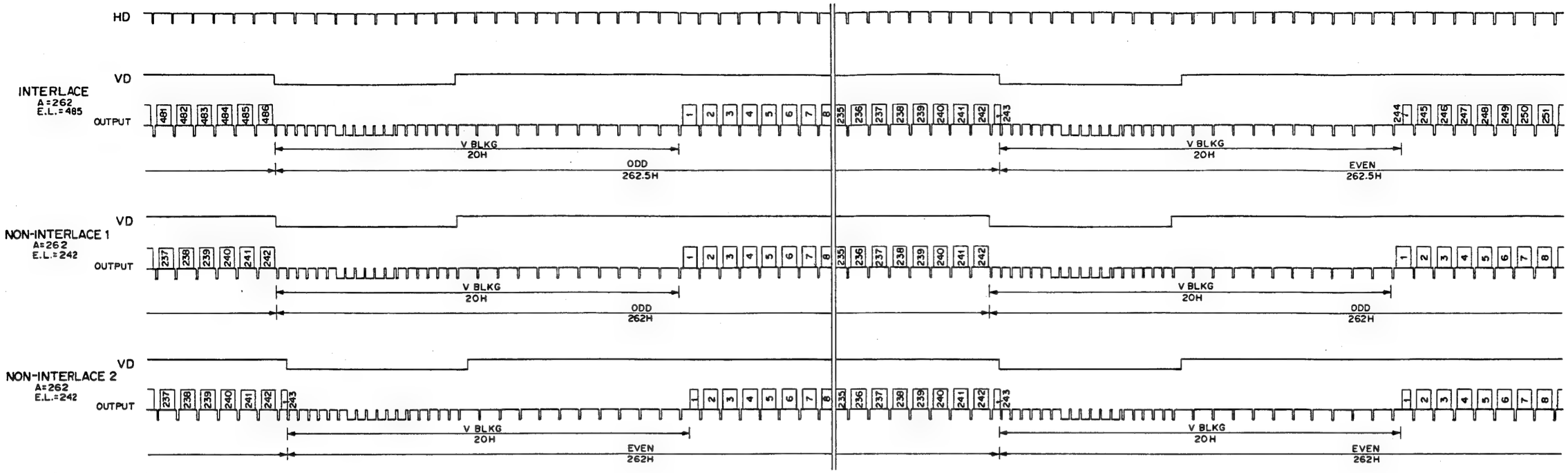
**Explanation of the timing chart**

Figure 3 is the timing charts for each operation mode. The details of these timing charts are given below:

- Frame integration interlace mode
  The R.R requires four pulses. Set the period of the R.R to (A + 1/2)H. A is an integer, 244 to 1023. It is 262 in the figure.
  Shooting information during STORAGE 1 and STORAGE 2 is output in the intervals of IMAGING C (ODD) and IMAGING D (EVEN). The CCD is reset in the intervals of IMAGING A and IMAGING B. Therefore, signals output during these intervals are meaningless.

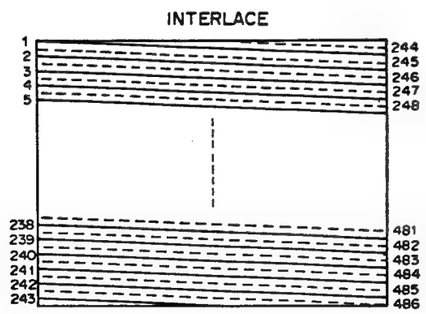
- Field integration interlace mode
  The R.R requires three pulses. Set the period of the R.R to (A + 1/2)H. A is an integer, 244 to 1023. It is 262 in the figure.
  Shooting information during STORAGE 1 and STORAGE 2 is output in the intervals of IMAGING B (ODD) and IMAGING C (EVEN). The CCD is reset in the interval of IMAGING A; therefore, signals output during this interval are irrelevant.

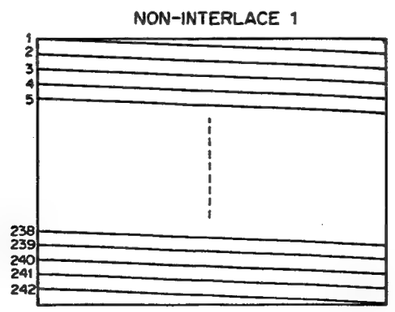
- Non-interlace mode
  The R.R requires two pulses regardless of the storage mode. Set the period of the R.R to A H. A is an integer, 244 to 1023. It is 262 in the figure.
  Shooting information in STORAGE 1 is output in the interval of IMAGING B. The CCD is reset in the interval of IMAGING A; therefore, signals output during this period are irrelevant.

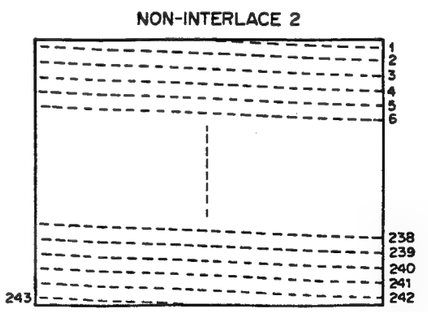



Note: EL means effective line

注意：E.L.は有効ライン数です。

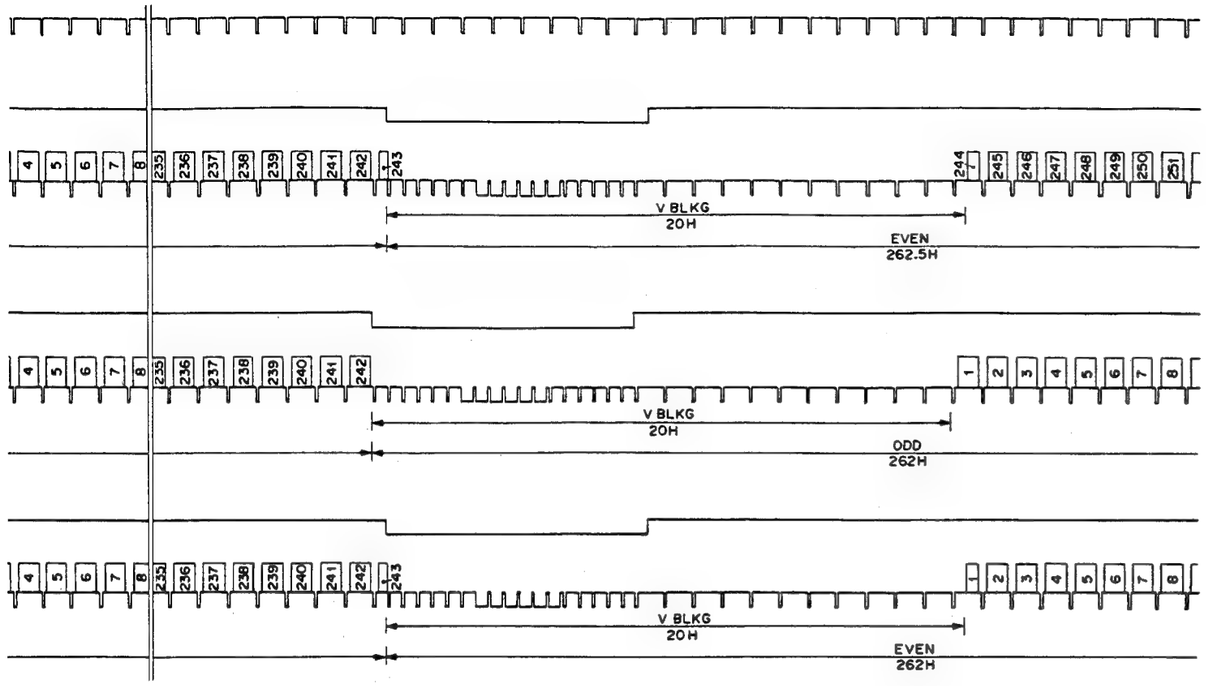


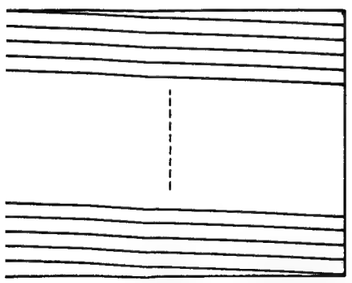




[Fig. 1]

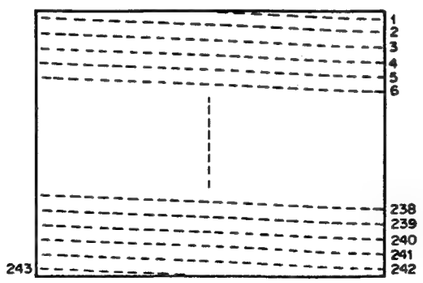
| Read out mode set | |
|---|---|
| Scanning mode | |
| Scanning | NORMAL MOD |
| | INVERSE MODI |
| Storage time and VIDEO OUT correla | |
| Vertical effective (TV lines) | |
| RESTART RESE | |
| Features and application | |




NON-INTERLACE 1

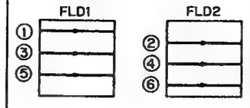
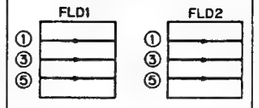
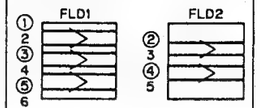
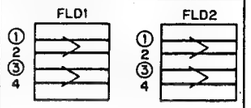
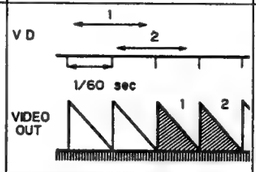
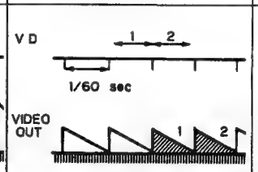
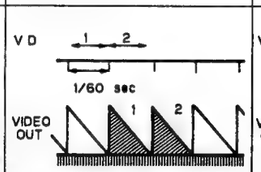
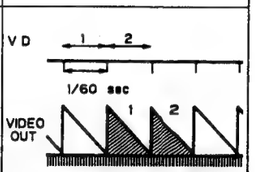
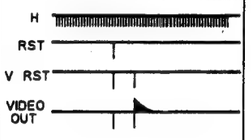


NON-INTERLACE 2

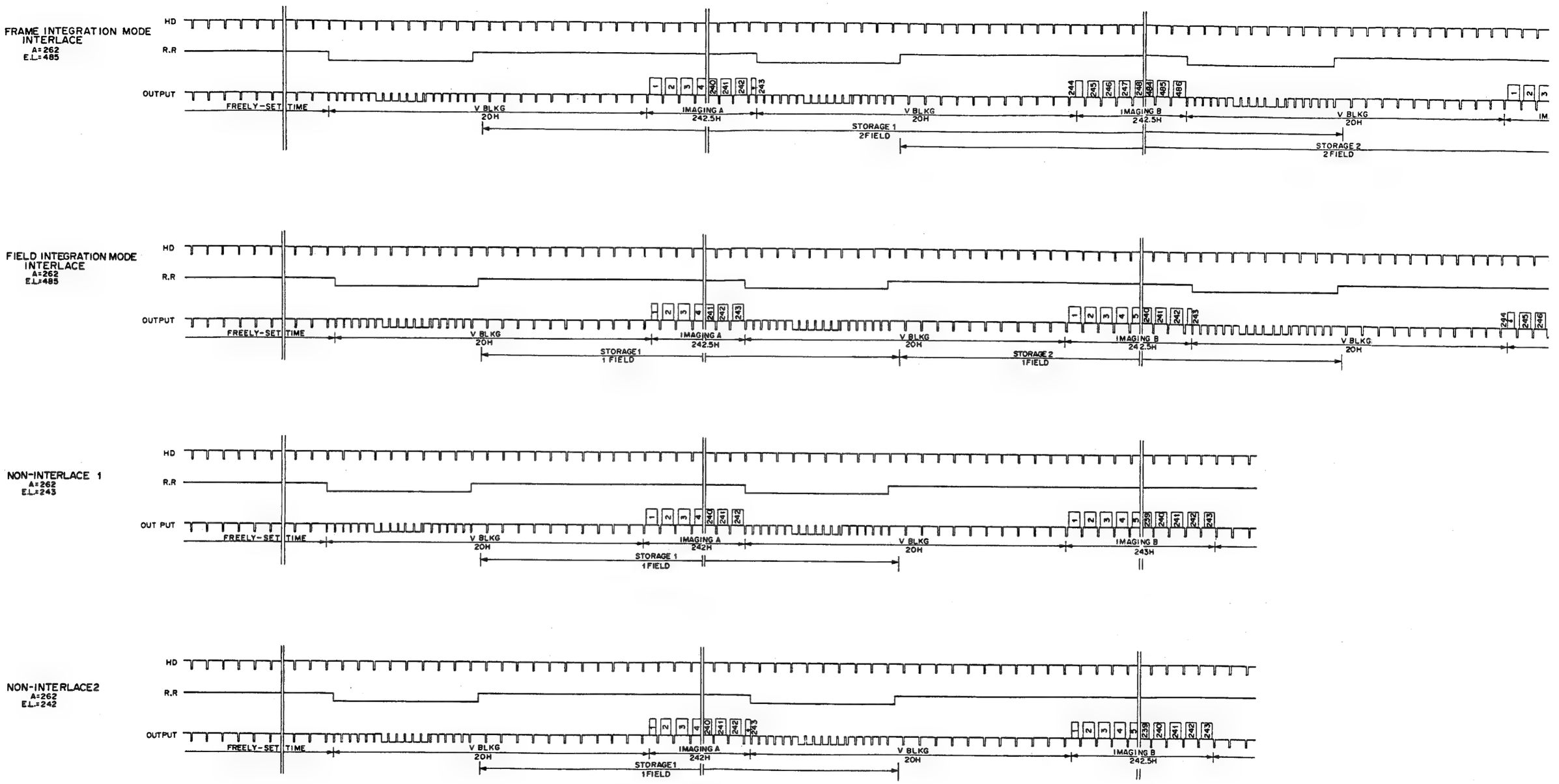



[Fig. 1]

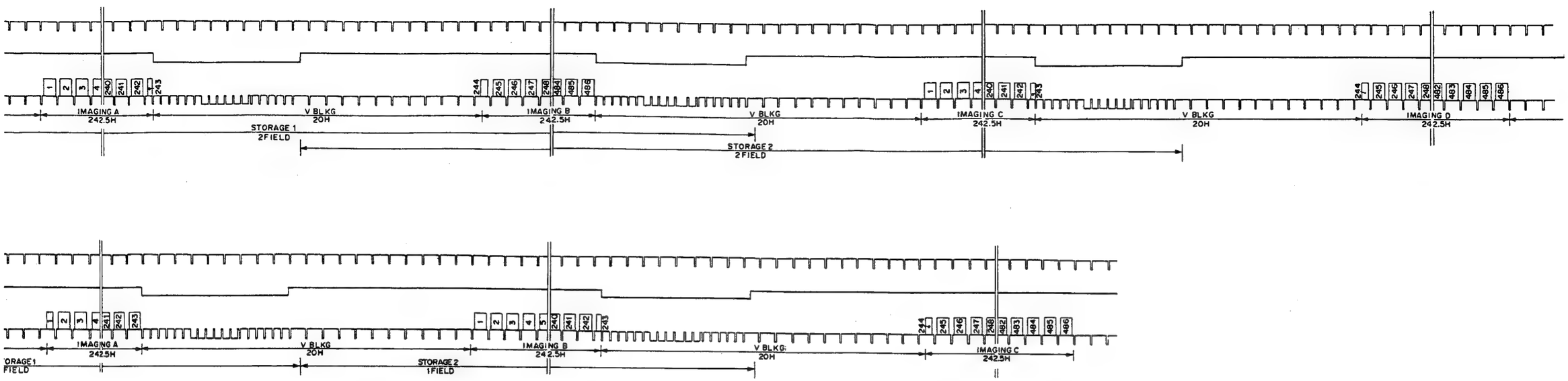


| Read out mode setting | | Frame integration mode (XC-75 initial setting) | | Field integration mode | |
|---|---|---|---|---|---|
| Scanning mode | | Interlace | Non-interlace | Interlace | Non-interlace |
| Scanning | NORMAL MODE |  |  |  |  |
| | INVERSE MODE | FLD 1 and FLD 2 are inverted. | FLD 1 and FLD 2 become ②, ④, ⑥.... | FLD 1 and FLD 2 are inverted. | FLD 1 and FLD 2 become ②, ④, ⑥.... |
| Storage time and VIDEO OUT correlation | |  |  |  |  |
| Vertical effective lines (TV lines) | | 485 | 242 | 350 | 242 |
| RESTART RESET | |  |  |  |  |
| Features and application | | As the highest possible resolution is obtained, it is adapted to the measurements of the frame memory. | Same system as XC-39. Operates per 1 vertical line. Note: The operation is field integration mode. | Due to the storage of 1/60 seconds, a picture with even less disturbances than the frame integration mode is obtained. Adapted to pick up a moving object. | This system obtains all the vertical information without decreasing the sensitivity in non-interlace mode. |

[Fig. 2] Relation between scanning mode and integration mode


FRAME INTEGRATION MODE
INTERLACE
A=262
E.L=485
HD
R.R
OUTPUT
FREELY-SET TIME
V BLKG
20H
IMAGING A
242.5H
STORAGE 1
2FIELD
V BLKG
20H
IMAGING B
242.5H
STORAGE 2
2FIELD
V BLKG
20H
FIELD INTEGRATION MODE
INTERLACE
A=262
E.L=485
HD
R.R
OUTPUT
FREELY-SET TIME
V BLKG
20H
STORAGE1
1 FIELD
IMAGING A
242.5H
V BLKG
20H
STORAGE 2
1FIELD
IMAGING B
242.5H
V BLKG
20H
NON-INTERLACE 1
A=262
E.L=243
HD
R.R
OUT PUT
FREELY-SET TIME
V BLKG
20H
STORAGE 1
1FIELD
IMAGING A
242H
V BLKG
20H
IMAGING B
243H
NON-INTERLACE2
A=262
E.L=242
HD
R.R
OUTPUT
FREELY-SET TIME
V BLKG
20H
STORAGE1
1FIELD
IMAGING A
242H
V BLKG
20H
IMAGING B
242.5H

[Fig. 3]


IMAGING A
242.5H
V BLKG
20H
IMAGING B
242.5H
V BLKG
20H
IMAGING C
242.5H
V BLKG
20H
IMAGING D
242.5H
STORAGE 1
2FIELD
STORAGE 2
2FIELD
IMAGING A
242.5H
V BLKG
20H
IMAGING B
242.5H
V BLKG
20H
IMAGING C
242.5H
ORAGE 1
FIELD
STORAGE 2
1FIELD
IMAGING A
242H
V BLKG
20H
IMAGING B
243H
STORAGE 1
1FIELD
IMAGING A
242H
V BLKG
20H
IMAGING B
242.5H
STORAGE1
1FIELD

[Fig. 3]

## 2-5. OPERATION MODE SETTING

The operation mode of the XC-73/75 can be selected as required.
Each mode is set using a switch or soldering jumper.

| No. | Item | Location | Setting | Factory-setting mode |
|---|---|---|---|---|
| 1 | γ correction mode | PR-165 Board | Jumper JR1, JR2*1 | OFF |
| 2 | Electronic shutter mode | MB-403 Board | Jumper JR1 | OPEN(NORMAL) |
| 3 | Shutter control pulse setting | MB-403 Board | Jumper JR2 | OPEN |
| 4 | Normal electronic shutter speed setting | MB-403 Board | Switch S1 | "0"(OFF) |
| 5 | Charge accumulation mode | MB-403 Board | Jumper JR3 | OPEN(FRAME) |
| 6 | Sync signal input/output (HD/VD) | SG-199 Board | Switch S1 | EXT(INPUT) |
| 7 | EXT-HD termination (ON/OFF) | SG-199 Board | Switch S2 | ON |
| 8 | EXT-VD termination (ON/OFF) | SG-199 Board | Switch S3 | ON |
| 9 | H phase advance* | SG-199 Board | Jumper JR1 to 6 | Only JR1 and JR2 are short circuit. |
| 10 | RESTART-RESET mode* | SG-199 Board | Jumper JR7, 8 | SHORT(OFF) |
| 11 | FIELD INVERT mode* | SG-199 Board | Jumper JR9 | OPEN |
| 12 | GAIN mode | Rear panel | Switch | FIX |
| 13 | MANUAL GAIN | Rear panel | Volume control | 0 dB |
| 14 | Clock signal output | Rear panel | Jumper JR1 | OPEN |

* : The H phase advance, restart-reset, and field inversion can be set in only the external sync mode.
Each operation mode is described below.

*1 : In case the board suffix -11 of PR-165 board, the switch S1 mounted insted of JR1 and JR2.
Serial number ;
XC-73 (UCJ) : 10001-15550
XC-75 (UCJ) : 10001-60900

**1. γ correction mode ( γ ON/ γ OFF)**

A γ - corrected video signal is output when the γ correction mode is set to ON.

No γ correction is performed when this mode is set to OFF. Therefore, a video output signal proportional to the light intensity of an object can be obtained.

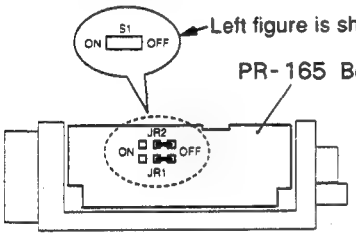
This correction mode is set using *internal jumpers JR1 and JR2 PR-165 board.

* In case the board suffix -11 of PR-165 board, the γ correction mode is set using slide switch S1.
  Serial number ;
  XC-73 (UCJ) : 10001-15550
  XC-75 (UCJ) : 10001-60900

It is set to γ OFF at the factory.

PR-165 board

| Mode | JR1, JR2 | S1 | input/output characteristic |
|---|---|---|---|
| γ ON (0.45) | ON : Short between the center land and the ON-side land. | ON | OUT / IN |
| γ OFF (1.0) | OFF : Short between the center land and the OFF-side land. | OFF | OUT / IN |

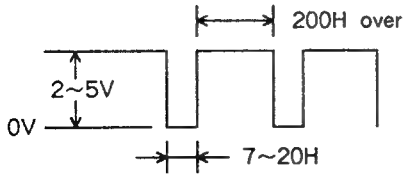



**2. Electronic shutter mode (NORMAL/SPECIAL)**

The electronic shutter mode sets the type of a CCD's electronic shutter.

- The NORMAL mode indicates an ordinary electronic shutter. The shutter speed is set using rotary switch S1 on the MB - 403 board (described in No. 4).
- The SPECIAL mode indicates an electronic shutter that has an exposure start in random timing. An input pulse that determines the exposure start is selected using jumper land JR2 on the MB - 403 (described in No.3).

**Note)** Be sure to feed the two reset pulses to the 12-pin connector (pin7) after the power is just turned on.




| Mode | JR1(MB - 403) |
|---|---|
| NORMAL | OPEN |
| SPECIAL | SHORT |

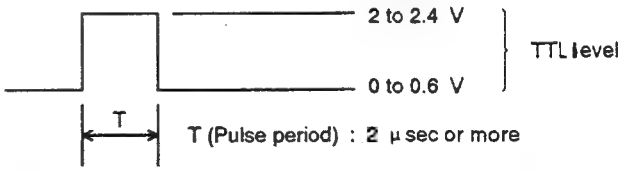
**3. Shutter control pulse setting**

This item selects an input pulse that determines the exposure start of an electronic shutter in the SPECIAL mode. VD and TR can be selected.

- If VD is selected, the falling edge of an internal VD pulse becomes the phase of a last shutter pulse just before an exposure start. Therefore, the exposure starts after about 2.0 μsec from this phase. The shutter speed is set according to the type and field of the CCD.
  (For the operation condition and timing chart, refer to the attached sheet.)
- If TR is selected, the rising edge of a pulse input from the 6 - pin connector (pin 2) on the rear panel becomes the phase of a last shutter pulse just before an exposure start. Therefore, the exposure starts after about 2.0 μ sec from this phase.
  The shutter speed is determined by the phase difference between the input pulse above and external sync VD pulse. It can be set freely.
  (For the operation condition and timing chart, refer to the attached sheet.)
- Controlling the shutter speed of an electronic shutter from the outside
  Set the electronic shutter mode to SPECIAL and set the input pulse to TR. In the state above, set switch S1 on the SG - 199 board (described later) to INT and extract an internal HD/VD output pulse from the camera. A control pulse is generated using this pulse. The shutter speed can be set from the outside when the generated control pulse is input to the 6 - pin connector (pin 2) on the rear panel.

**[Specification of shutter control pulse]**

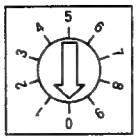
Input to a 6 - pin connector (pin 2) on the rear panel.




**4. Normal electronic shutter speed setting**

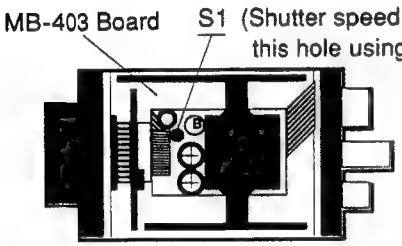
This item sets the electronic shutter speed in the NORMAL mode or sets the flicker - less mode. The electronic shutter speed and flicker - less mode are set using rotary code switch S1 on the MB - 403 board.

| Position | Shutter speed |
|---|---|
| 0 | OFF |
| 1 | 1/125 |
| 2 | 1/250 |
| 3 | 1/500 |
| 4 | 1/1000 |
| 5 | 1/2000 |
| 6 | 1/4000 |
| 7 | 1/10000 |
| 8 | Flicker-less mode* |
| 9 | Flicker-less mode* |



Switch (S1) on the MB-403 board (Factory setting)

* : The flicker-less mode can be set when the rotary code switch is set to position 8 or 9. In positions 8 and 9, the shutter speed is 1/100 sec for EIA, and 1/120 sec for CCIR.




*Confirmation of Electronic Shutter OFF Position while Monitoring

**Condition:** Fix the lens iris.

Either of the two methods, described in a) and b) respectively, can be used to perform this confirmation.

a) Turn the rotary switch S1 on the MB-403 board clockwise and stop it where the image becomes brightest on the monitor. This detect position is the Shutter OFF position.

b) Turn the rotary switch S1 on the MB-403 board in the clockwise direction until the brightness of the image remains unchanged over two consecutive positions. Turn the switch one position farther. This is the shutter OFF position.

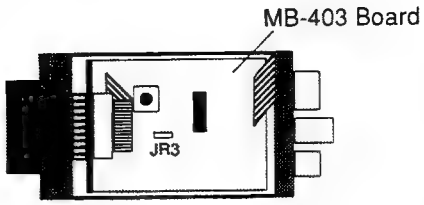
**5. Charge accumulation mode**

The accumulation mode sets the period in which signal charges are read from a CCD photosensor.

The accumulation mode is set using a jumper land JR3 (FLD) on the MB-403 board. FLD is set to FIELD when it is short circuit. FLD is set to FRAME when it is opened.

- When the accumulation mode is set to FIELD, it enters the field accumulation mode in which signal charges are simultaneously read from the pixels in group 2.
- When the accumulation mode is set to FRAME, it enters the frame accumulation mode in which signal charges are alternately read from the pixels in group 2.
- In the frame accumulation mode, the sensitivity during noninterlaced scanning is one half of that during interlaced scanning. (Refer to Fig. 2 on page 2-11.)

The accumulation mode is set to FRAME at the factory.




**6. Sync signal input/output (HD/VD)**

This item sets whether a sync signal is output to the outside or input from the outside.

The external and internal sync modes are set using switch S1 on the SG-199 Board.

To set EXTERNAL mode, set switch S1 to the "E" side.

To set INTERNAL mode, set it to the "I" side

In case the board suffix -11 and -12 of SG-199 board, "EXT" and "INT" are printed on the board.

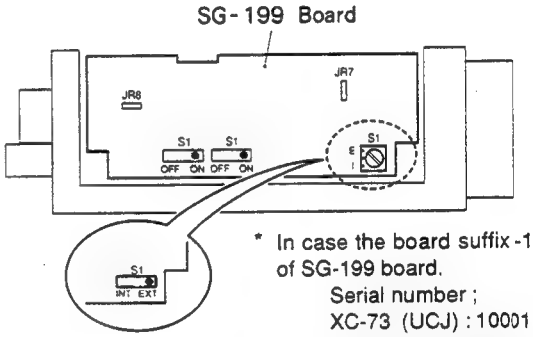
Serial number

XC-73 (UCJ) : 10001-15750

XC-75 (UCJ) : 10001-63900

- A video output signal synchronized with the sync signals (HD and VD signals) input from the outside is odtained when EXTERNAL (internal sync mode) is set.
- A sync signal that is generated internally can be output to the outside when INTERNAL (internal sync mode) is set.

Factory setting is EXTERNAL (external sync mode) .




* In case the board suffix -11 and -12 of SG-199 board.

Serial number ;

XC-73 (UCJ) : 10001-15750

XC-75 (UCJ) : 10001-63900

Changing the external sync input impedance

| * For high impedance input | | |
|---|---|---|
| SG-199 board | | |
| S2 | OFF | HD signal |
| S3 | OFF | VD signal |

Outputting the internal sync signals "HD" and "VD"

| SG-199 board | | |
|---|---|---|
| S1 | INT | |
| S2 | OFF | HD signal |
| S3 | OFF | VD signal |

### 7. EXT-HD termination (ON/OFF)

The HD input signal from the outside is terminated in 75 ohms. The 75ohm termination is set using switch S2 on the SG-199 board. To terminate in 75 ohms, set switch S2 to ON. If not so, set switch S2 to OFF.

**Notes :** If switch S2 is set to OFF, a high impedance of more than 100K ohms is received.
To get the HD output signal, set switch S2 to OFF.

### 8. EXT-VD termination (ON/OFF)

The VD input signal from the outside is terminated in 75 ohms. The 75ohm termination is set using switch S3 on the SG-199 board. To terminate in 75 ohms, set switch S3 to ON. If not so, set switch S3 to OFF.

**Notes :** If switch S3 is set to OFF, a high impedance of more than 100K ohms is received.
To get the VD output signal, set switch S3 to OFF.

### 9. H phase advance

The phase of an internally generated HD signal can be advanced relative to the phase of an HD signal input from the outside during external HD/VD synchronization. The phase advance is set using jumper lands JR1 through JR6 on the SG-199 board.

| Jumper land | H phase advance |
|---|---|
| JR1 | 1 bit |
| 2 | 2 |
| 3 | 4 |
| 4 | 8 |
| 5 | 16 |
| 6 | 32 |

1 bit ≒ 70 ns

**Example :** A phase advance of 1 μsec is obtained by the expression below.
1000 ns ÷ 70=14.3

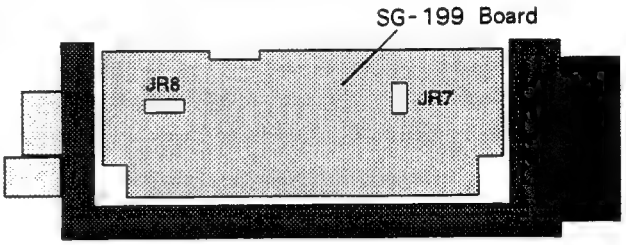
- In this case, if jumper lands JR2 through JR4 are short-circuited, the phase advance below can be set.
  2+4+8=14 bit × 70=980 ns=0.98 μs
- If jumper lands JR1 through JR4 are short-circuited, the phase advance below can be set.
  1+2+4+8=15 bit × 70=1050 ns=1.05 μs

Jumper lands JR1 and JR2 are set to the short-circuit state at the factory.

### 10. RESTART/RESET mode (R.R mode)

The RESTART/RESET mode fetches one-screen information in the external sync mode at any time.
The RESTART/RESET mode is set using jumper lands JR7 and JR8 on the SG-199 board.

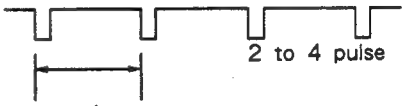
| Jumper land | NORMAL | R.R |
|---|---|---|
| JR7 | SHORT | OPEN |
| JR8 | SHORT | OPEN |




External sync input signal is required if the R.R mode is selected. The video signal is output by adding the HD signal to pin 6 of 12-pin connector and the R.R signal to pin 7 respectively.

**Conditions : HD/R.R level 2 to 5Vp-p**
Frequency(period)
HD signal : 15.734 kHz ± 1% (63.56 μs ± 1%)
Continuous pulse

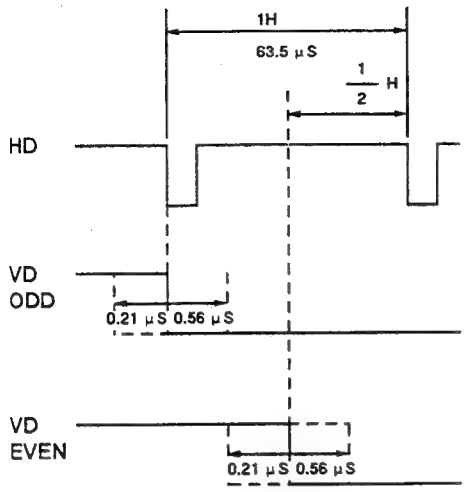

VD signal : 244 to 1023 1/2 H
2 to 4 pulses (depending on the mode)




Any time interval $244 \sim 1023\frac{1}{2}$ H

- The HD pulse is input continuously.
- The VD pulse can be input in any timing if the phase relation between the VD and HD pulses meets the specification (below).

• Phase




• For the phase relation between external input HD and VD pulses, the allowance for the center phase in the specification is +8 clocks and - 3 clocks (maximum) as shown in the figure above.
Jumper lands are set to NORMAL at the factory.

| FRAME accumulation | | FIELD accumulation | |
|---|---|---|---|
| interlaced | non-interlaced | interlaced | non-interlaced |
| R.R pulse | | | |
| 4 | 2 | 3 | 2 |

### 11. FIELD INVERT mode

The FIELD INVERT mode sets the field inversion of a video output signal when an external sync signal is input.
The FIELD INVERT mode is set using jumper land JR9 on the SG - 199 board. It is set to INVERSE when JR9 is short- circuited, and set to NORMAL when JR9 is opened.

- If the FIELD INVERT mode is set to INVERSE, the field of the video output signal is inverted for the external sync signal. An even signal is output when the field of the external sync signal is odd. An odd signal is output when it is even.
- If the FIELD INVERT mode is set to NORMAL, the field of the video output signal is the same as during ordinary external synchronization. An odd signal is output when the field of the external sync signal is odd. An even signal is output when it is even.

The FIELD INVERT mode is set to NORMAL with JR9 opened at the factory.

### 12. GAIN mode (AUTO/FIX/MANUAL)

The GAIN mode sets the gain of a video output signal.
If the GAIN mode is set to AUTO, an automatic gain control (AGC) function is activated. The maximum gain of the automatic gain control is +18 dB.
In the MANUAL mode, the gain can be changed in the range of 0 to +18 dB using the volume control on the rear panel.

| Display | Mode |
|---|---|
| A | AUTO GAIN |
| F | FIX GAIN |
| M | MANUAL GAIN |

The GAIN mode is set to FIX GAIN at the factory.

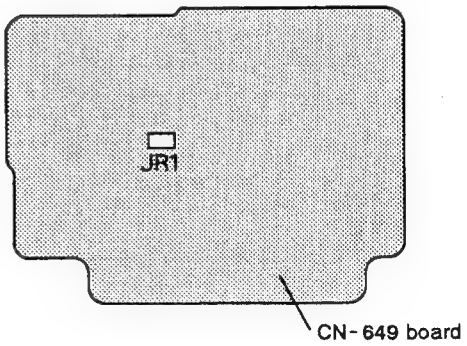
### 13. MANUAL GAIN control

The gain of a video output signal can be changed when the GAIN mode described above is set to MANUAL GAIN.
Minimum : 0 dB
Maximum : +18 dB
The gain of the video output signal is set to 0 dB at the factory.

### 14. CLOCK OUTPUT MODE

To obtain the clock signal output, short-circuit the jumper land JR1 on the CN-649 board.
The clock signal is output at pin 9 of 12-pin camera connector.

| Output Level | 5Vp-p |
|---|---|
| Output Impedance | 75 Ω |



## SPECIAL mode setting (1)

| | Fixed | Optional |
|---|---|---|
| Timing | ○ | – |
| Speed | ○ | – |

● To set up the SPECIAL mode setting (1) , confirm or set the jumper lands according to the following tables.
(A figure showing the board locations of the jumpers necessary for the special mode setting is given on page 2-25 (E) .)

● MB-403 Board

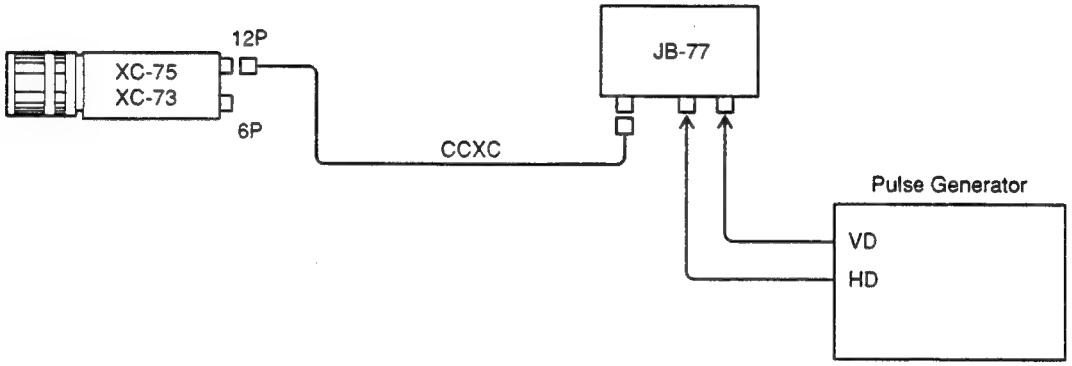
| | |
|---|---|
| JR1 | SHORT |
| JR2 | SHORT(VD) |
| JR3* | SHORT |

● SG-199 Board

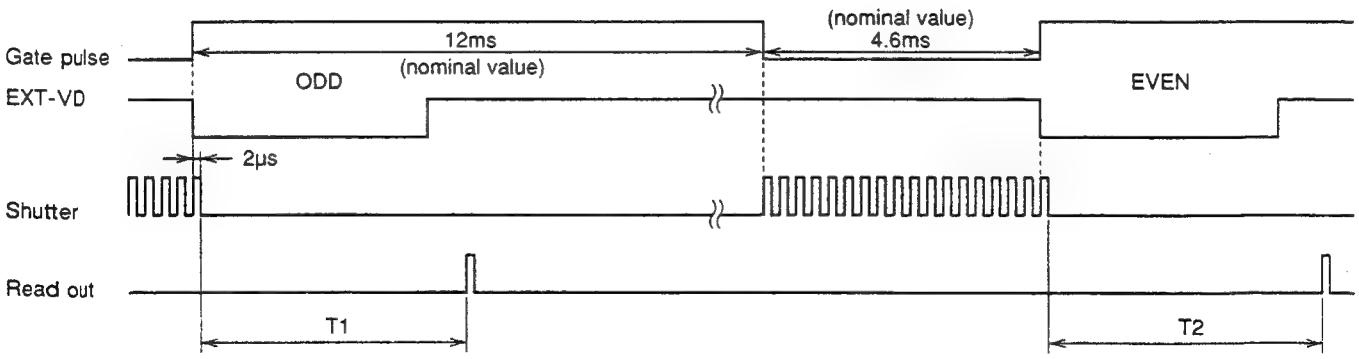
| | |
|---|---|
| S1 | EXT |
| JR7 | SHORT |
| JR8 | SHORT |

* When jumper land is shorted, FIELD mode is available. When jumper land is opened, FRAME mode is available, but the sensitivity becomes half level.

● Connection




● Pulse timing chart




| STANDARD | FIELD | EXPOSURE TIME | SHUTTER SPEED |
|---|---|---|---|
| EIA | T1 | 9H+42.2 μs | 1/1630 s |
| | T2 | 8.5H+42.2 μs | 1/1720 s |
| CCIR | T1 | 14.5H+43.3 μs | 1/1030 s |
| | T2 | 14H+43.3 μs | 1/1070 s |

**SPECIAL mode setting (2)**

| | Fixed | Optional |
|---|---|---|
| Timing | – | ○ |
| Speed | ○ | – |

- To set up the SPECIAL mode setting (2) , confirm or set the jumper lands according to the following tables.
  When this setting is executed, camera mode is changed to R.R mode from normal mode.
  (A figure showing the board locations of the jumpers necessary for the special mode setting is given on page 2-25 (E) .)

- MB-403 board

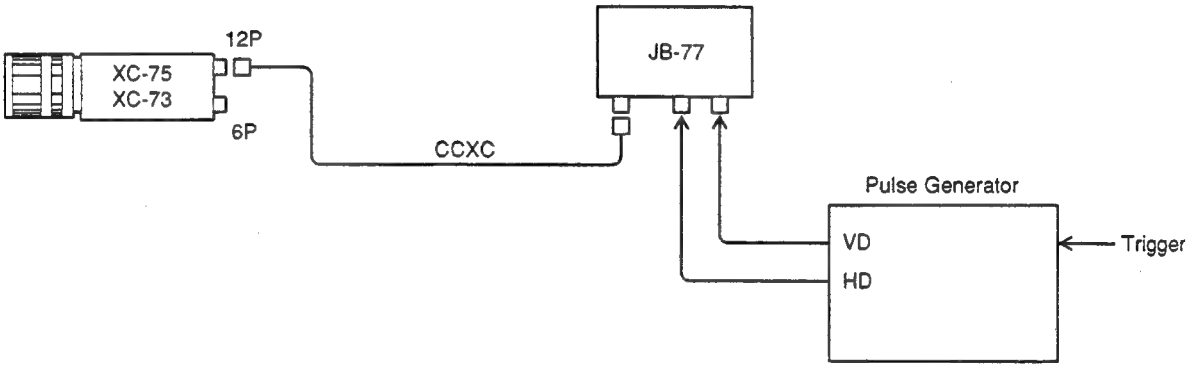
| | |
|---|---|
| JR1 | SHORT |
| JR2 | SHORT(VD) |
| JR3* | SHORT |

- SG-199 Board

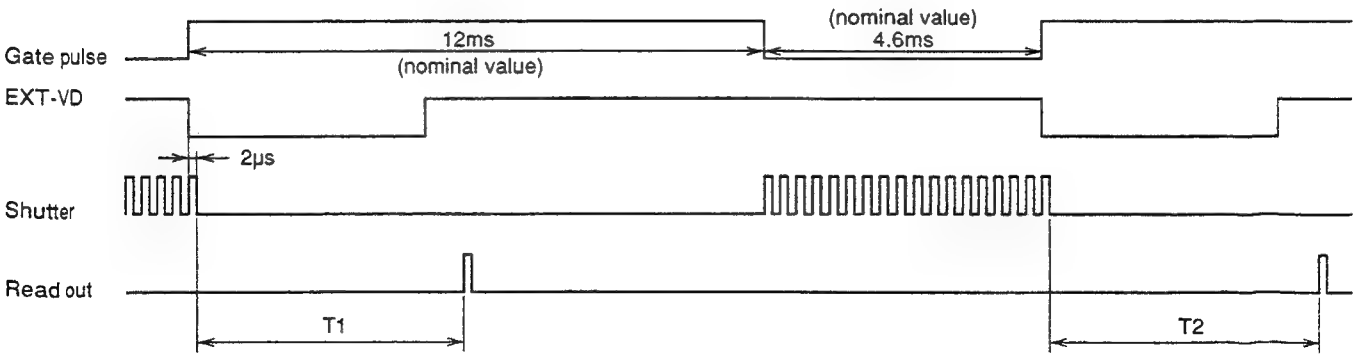
| | |
|---|---|
| S1 | EXT |
| JR7 | OPEN |
| JR8 | OPEN |

* When jumper land is shorted, FIELD mode is available. When jumper land is opened, FRAME mode is available, but the sensitivity becomes half level.

- Connection




- Pulse timing chart




- For more details of T1, refer to SPECIAL mode setting (1).
- A VD pulse must be latched by an HD pulse because of the R.R mode.

**SPECIAL mode setting (3)**

| | Fixed | Optional |
|---|---|---|
| Timing | – | ○ |
| Speed | – | ○ |

- To set up the SPECIAL mode setting (3) , confirm or set the jumper lands according to the following tables.
  When this setting is executed, camera mode is changed to R.R mode from normal mode.
  (A figure showing the board locations of the jumpers necessary for the special mode setting is given on page 2-25 (E) .)

- MB-403 Board

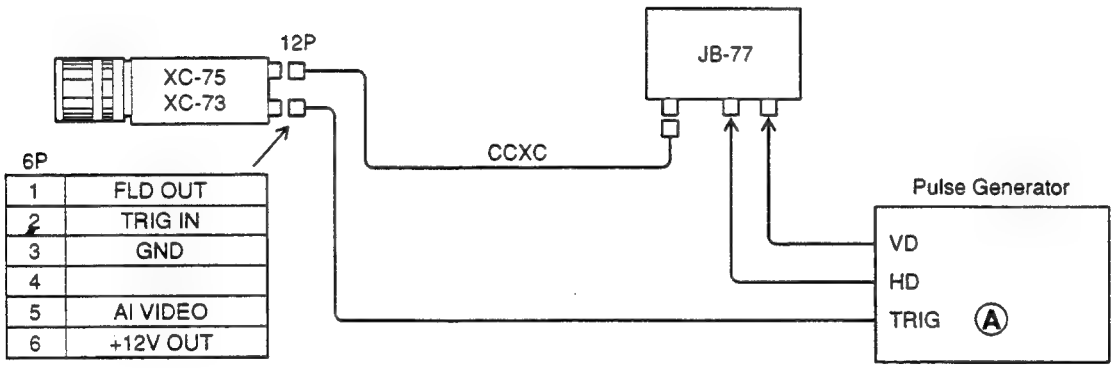
| | |
|---|---|
| JR1 | SHORT |
| JR2 | SHORT(TR) |
| JR3* | SHORT |

- SG-199 Board

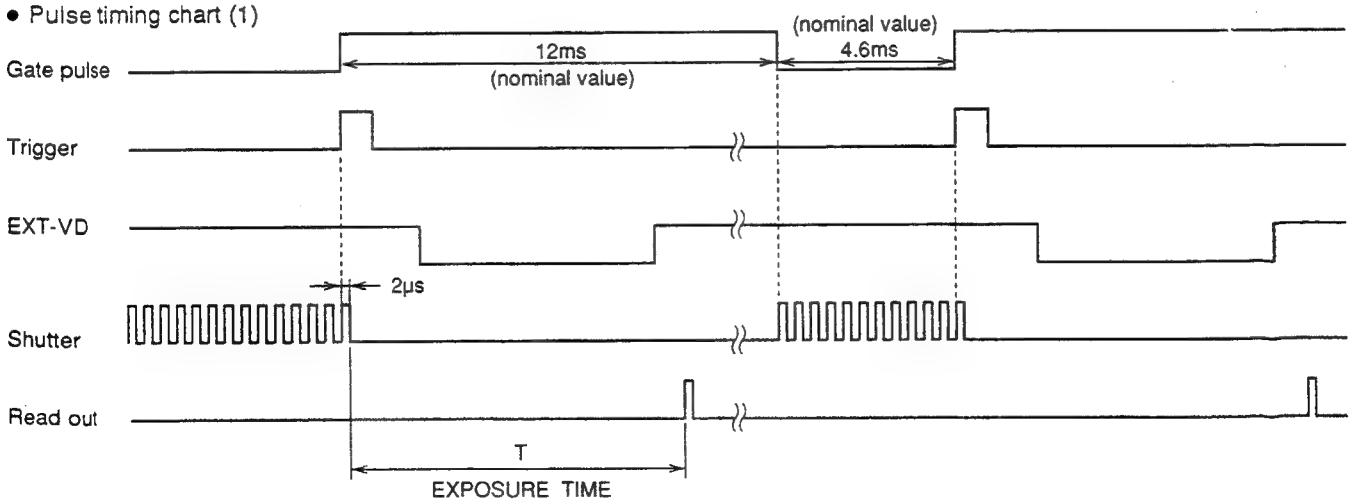
| | |
|---|---|
| S1 | EXT |
| JR7 | OPEN |
| JR8 | OPEN |

* When jumper land is shorted, FIELD mode is available. When jumper land is opened, FRAME mode is available, but the sensitivity becomes half level.

- Connection

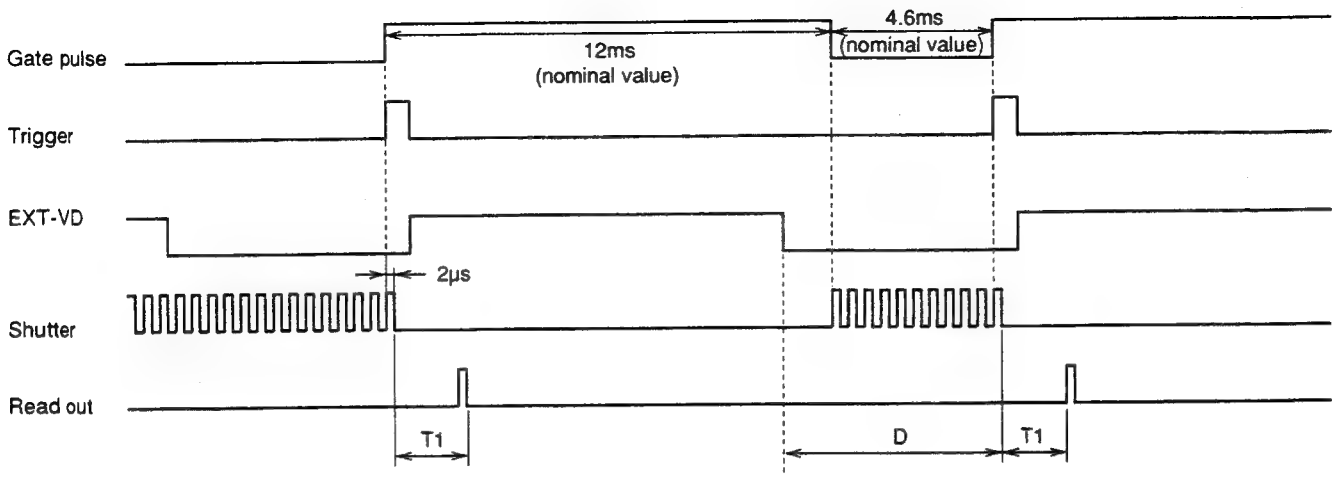



- Pulse timing chart (1)



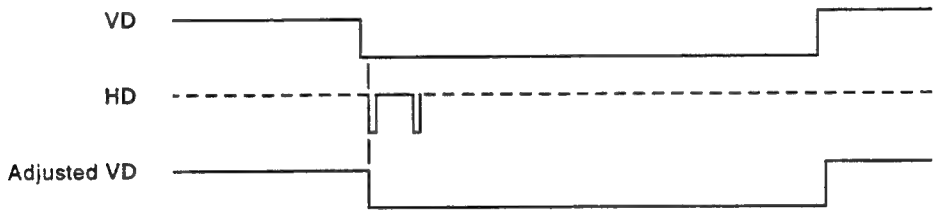

| STANDARD | FIELD | EXPOSURE TIME | SHUTTER SPEED |
|---|---|---|---|
| EIA | ODD | MAX 13 ms | 1/77 s |
| CCIR | EVEN | MAX 13 ms | 1/77 s |

● Pulse timing chart (2)




| STANDARD | FIELD | EXPOSURE TIME | SHUTTER SPEED |
|---|---|---|---|
| EIA | ODD | MIN 2 μs | 1/500000 s |
| CCIR | EVEN | MIN 2 μs | 1/500000 s |

**Notes :** 1. Adjust the VD pulse to the phase of the HD pulse because of the R.R mode.




2. For the shutter using an arbitray trigger, a VD pulse is usually generated after a trigger pulse. The maximum shutter speed below is thus obtained.
   EIA : 1/1548 s
   CCIR : 1/997 s
3. The extra-high shutter speed below id obtained when a trigger pulse is delayed relative to a VD pulse.

| STANDARD | FIELD | EXPOSURE TIME | SHUTTER SPEED |
|---|---|---|---|
| EIA | T1 | (9H+42.2 μ s) - D | MIN 1/500000 s |
| CCIR | T1 | (14.5H+43.3 μ s) - D | MIN 1/500000 s |

D : Delay of trigger pulse relative to VD pulse.

**SPECIAL mode setting (4)**

(Application of a shutter speed to the external control)

To set up the SPECIAL mode setting (4) , confirm or set the jumper lands according to the following tables.
(A figure showing the board locations of the jumpers necessary for the special mode setting is given on page 2-25 (E) .)

• MB-403 Board

| | |
|---|---|
| JR1 | SHORT |
| JR2 | SHORT(TR) |
| JR3* | SHORT |

• SG-199 Board

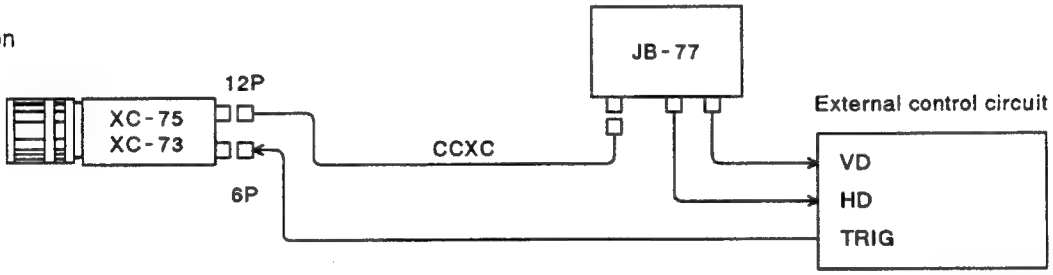
| | |
|---|---|
| S1 | INT |
| JR7 | SHORT |
| JR8 | SHORT |

• SG-199 Board

| | |
|---|---|
| S2 | OFF |
| S3 | OFF |

* When jumper land is shorted, FIELD mode is available. When jumper land is opened, FRAME mode is available, but the sensitivity becomes half level.

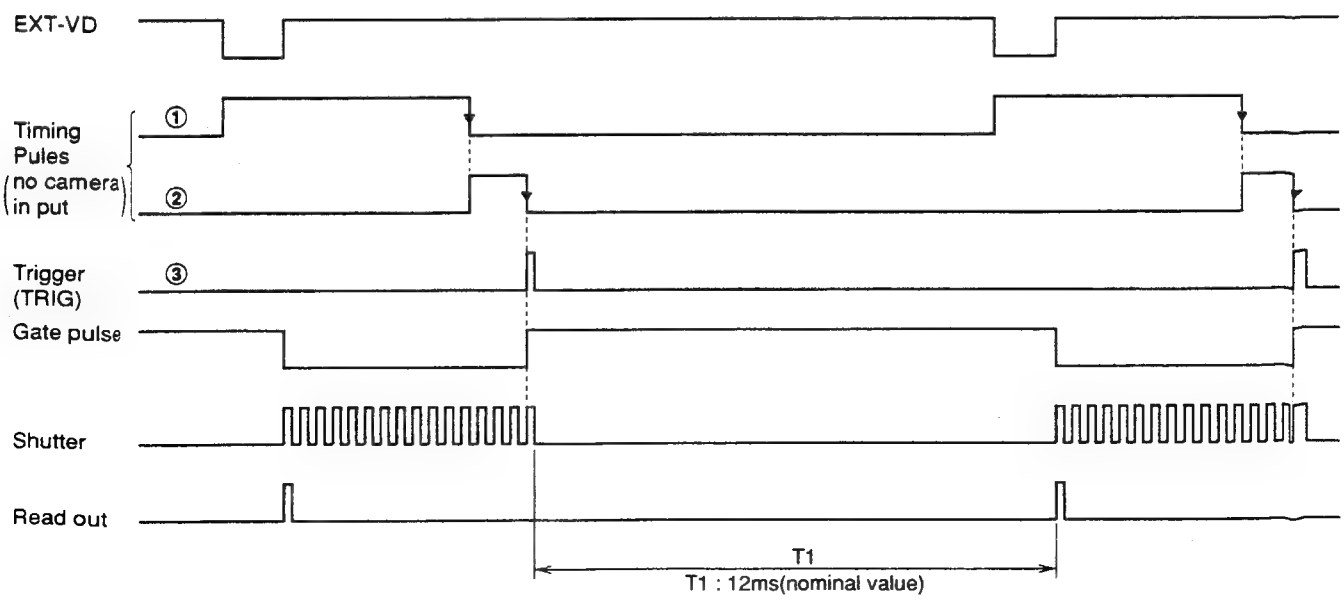
• Connection



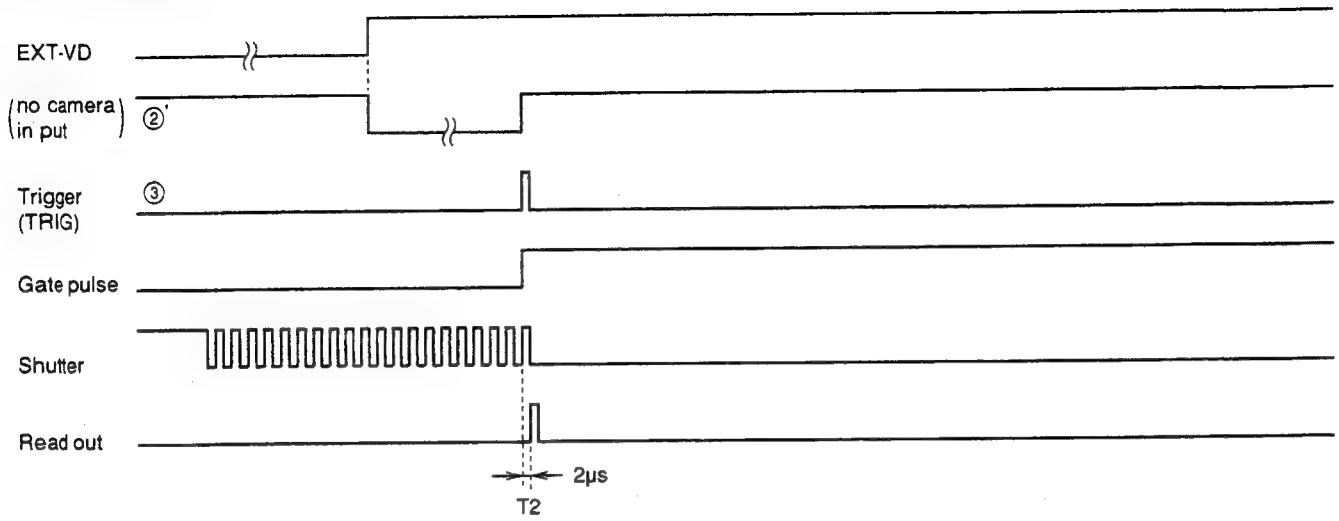

(A circuit generating TRIG pulse ③ by using timing pulses ①,② and ②' as shown below is needed.)

• Pulse timing chart (Exposure time : T1 through T2 can be changed continuously.)

Long time exposure

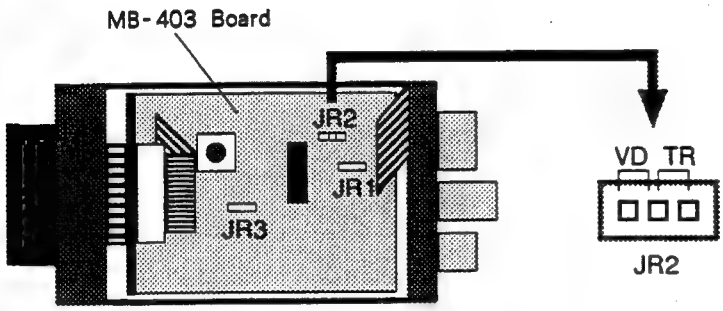


Short time exposure

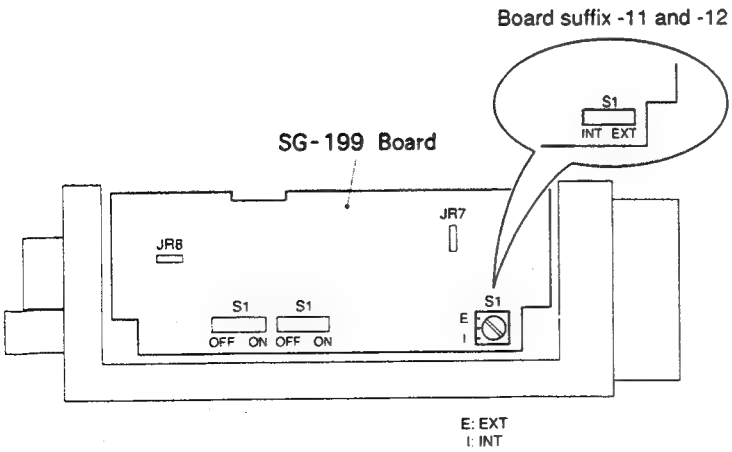



**BOARD LOCATION for SPECIAL mode setting**

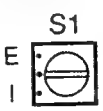
- MB-403 board




- SG-199 board




Note ;
Do not set S1 switch to mechanical center because that abnormal operation will be caused if S1 is set to mechanical center.




This is bad setting.

## 2-6. THEORY OF OPERATION

### 2-6-1. Operation Theory of CCD

A CCD (Charge-Coupled Device) image sensor consists of a regularly laid-out MOS (Metal-Oxide-Semiconductor) capacitor. The MOS capacitor has three basic functions below that treat a charge.

1. Photoelectric Conversion (Photosensor)
   When incident light falls on the MOS capacitor, the charge is generated in proportion to the illumination received.
2. Charge Storage
   When a voltage is applied to the electrode of a MOS capacitor, a "potential well" is generated in the silicon layer. The charge is stored in this well.
3. Charge Transfer
   When a higher voltage is applied to the electrode, a deeper well is generated. When a lower voltage is applied, a shallower well is generated.
   The charge is transferred using this characteristic. When a higher voltage is applied to the electrode, a deeper "potential well" is generated. The charges accumulated in an adjacent well flows into the "potential well". When this operation is sequentially repeated in the regularly laid-out electrode, the charge is transferred from one MOS capacitor to another MOS capacitor. This is the theory of the CCD charge transfer.

### 2-6-2. Structure of CCD Charge Transfer

In the interline transfer system that the XC-75 and the XC-73 use, the charge corresponding to the brightness of an image formed on a CCD image sensor is sequentially transferred as shown in Fig. 3 on page 2-27. The charge corresponding to the brightness of an object detected using a photosensor is first transferred to an adjacent vertical transfer register. The charge transferred to the vertical transfer register is sequentially transferred to a horizontal transfer register in the vertical direction. The charge transferred to the horizontal transfer register is sequentially transferred in the horizontal direction and output from the output stage.

**1. Vertical Transfer**

The vertical transfer register transfers a charge by four-phase driving. Fig.1 shows the state of a "potential well" at each time.

In the state of time t0, the electrode voltage is (V1 = V2) > (V3 = V4). Therefore, the well is deepened in the potentials of V1 and V2 with high voltage. The charge is stored in the deep well.

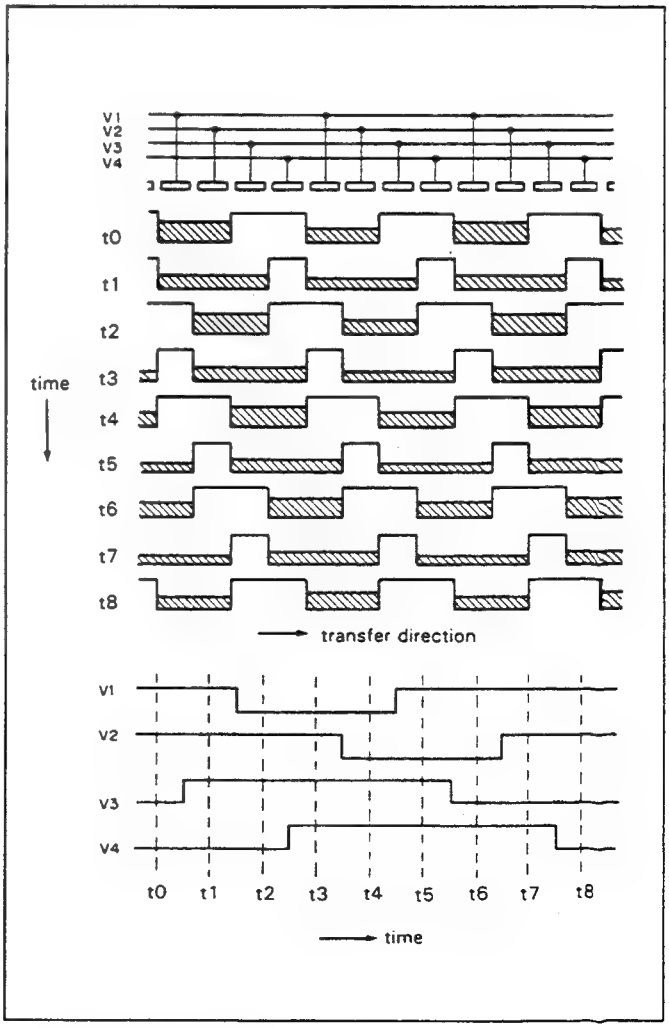
In time t1, the electrode voltage is (V1 = V2 = V3) > (V4). The charge is stored in the well of V1, V2, and V3.

In time t2, the electrode voltage is (V2 = V3) > (V4 = V1). The charge is stored in the well of V2 and V3.

The state of the electrode voltages in time t3 and later is described below.

| | |
|---|---|
| Time t3 | (V2 = V3 = V4) > (V1) |
| Time t4 | (V3 = V4) > (V1 = V2) |
| Time t5 | (V4) > (V1 = V2 = V3) |
| Time t6 | (V4 = V1) > (V2 = V3) |
| Time t7 | (V4 = V1 = V2) > (V3) |
| Time t8 | (V1 = V2) > (V3 = V4) |
| | (Same as the state of time t0.) |

This operation is sequentially repeated for the vertical transfer.




**[Fig. 1] Vertical Transfer**

## 2. Horizontal Transfer

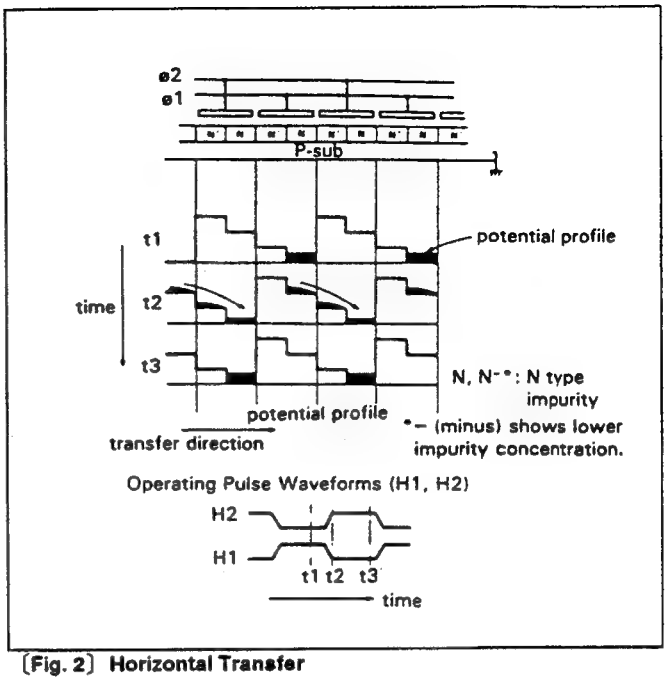
The horizontal transfer register transfers a charge by two-phase driving. Fig. 2 shows the state of a "potential well" at each time.

In the state of time t1, the electrode voltage is H1 > H2. Therefore, the well is deepened in the electrode of H1 with high voltage. The charge is stored in the deep well.

In the state of time t2, the voltage of H1 and H2 is inverted. The well of H2 becomes deep, and the well of H1 becomes shallow. The well of H2 becomes deeper than that of H1, so the signal charge flows into H2 with deeper well.

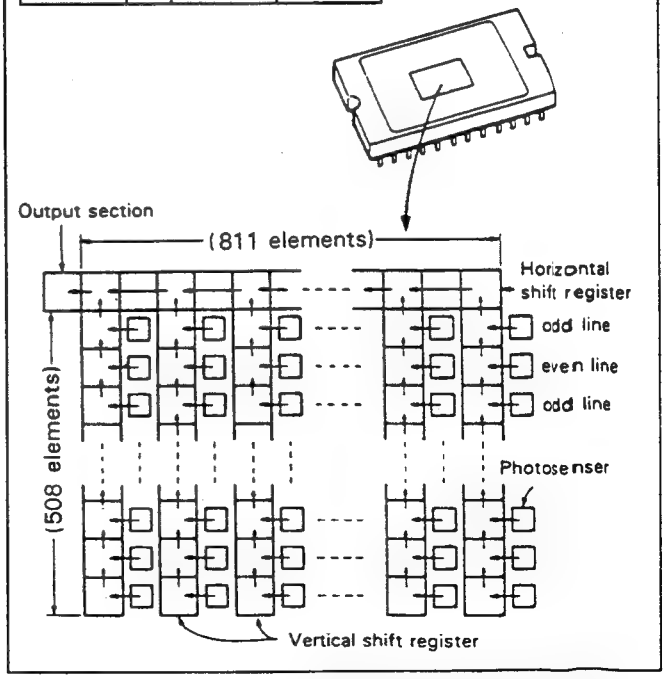
In the state of time t3, the electrode voltage does not change. The signal charge thus flows into the well of H2. One charge transfer is then completed.

This operation is sequentially repeated for horizontal transfer.




〔Fig. 2〕 **Horizontal Transfer**

| Standard | | Overall Picture Element | Effective Picture Element |
|---|---|---|---|
| EIA | H | 811 | 768 |
| | V | 508 | 494 |
| CCIR | H | 795 | 752 |
| | V | 596 | 582 |




〔Fig. 3〕 **The interline-transfer organization of the CCD image sensors**

### 2-6-3. PA-147 Board(XC-75)
### PA-152 Board(XC-73)

The light passed through a camera lens strikes against the chip surface of IC1 (CCD image sensor) on the PA board.
An approximately 400,000 photosensors are arrayed on the CCD surface, and the incident light is converted into the charge corresponding to the brightness of light in a photosensor block.
The converted charge is stored in the photosensor for storage time to be set, then read to the transfer register.
The charge sequentially transferred to the transfer register is lastly output to the output stage of IC1 to produce a CCD output signal.
The output signal of IC1 is input through buffer amplifier Q3 to IC2 (CDS IC), where the noise component of the CCD output signal is reduced by correlative double sampling.
The resultant signal is output in the level that is about two times as high as an input signal.
The SHP and SHD pulses input to IC2 are a sampling pulse for correlative double sampling. The signal output from IC2 is output through buffer amplifier Q1 from the PA board and sent to the MB-403 board.

### 2-6-4. MB-403 Board

The MB-403 board mounts a timing pulse generator for CCD control and the circuit blocks below.

a. Timing pulse generator
b. Clock drive circuit for CCD vertical transfer
c. Electronic shutter control circuit
d. CCD-VSUB voltage control circuit
e. PB-BIAS voltage control circuit
f. System clock generator
g. Clock output driver
h. Video signal output driver

a. Timing pulse generator

Timing pulse generator IC3 generates timing pulses required for CCD driving by inputting a 28 MHz clock from the system clock generator and inputting HD and VD signals from the SG-199 board.

| | |
|---|---|
| XPG | : Clock for CCD precharge gate |
| XH1, XH2, XLH1 | : Two-phase clock for CCD horizontal transfer |
| XV1 to XV4 | : Two-phase clock for CCD vertical transfer |
| XSUB | : Electronic shutter pulse |
| XSG1, XSG2 | : Charge read pulse from photosensor |

In addition, timing pulse generator IC3 generates the signal processing pulses below.

| | |
|---|---|
| SH1 | : Sampling pulse for correlative double sampling |
| SH2 | : Sampling pulse for correlative double sampling |
| CLP3 | : Clamp pulse for DC reproduction |

The timing pulse generator also outputs shutter pulse X-SUB whose generation period changes according to the output of rotary code switch S1, and sends it to the electronic shutter control circuit described later.

b. Clock drive circuit for CCD vertical transfer
Clock driver circuit for CCD vertical transfer IC1 inputs the CCD vertical transfer clock pulses (V1 through V4) from IC3 and the signal charge read pulses (SG1 and SG2) from a photosensor and outputs pulses V1 through V4 with SG1 and SG2 added to V1 and V3.
In this case, IC1 functions as the driver of pulses V1 through V4 so that it can directly drive the CCD.
The V2 output pulse is sent to a charge pump consisting of D1, D2, C1, and C2 to produce a V-SUB DC voltage (approximately +25 V).

c. Electronic shutter control circuit
The electronic shutter control circuit consisting of IC4, IC5, and IC6 switches the electronic shutter mode (NORMAL/SPECIAL) and controls the SPECIAL shutter.
Jumper land JR1 is set to OPEN at the factory. In this state, IC6 for a SPECIAL shutter is in the reset state.
For the output signal of a shutter pulse selection circuit consisting of IC5, a NORMAL shutter pulse, that is, the X-SUB output pulse of IC3 is selected.
The output logic of IC4 is inverted when jumper land JR1 is set to SHORT. The reset of IC6 is then canceled. IC6 can operate for the trigger pulse or VD pulse from the 6-pin connector on the rear panel in this case (the VD or trigger pulse is selected using jumper land JR2). Simultaneously, the output pulse of IC6 is selected as the output signal of a shutter pulse selection circuit consisting of IC5. This enables the operation of the SPECIAL shutter.
The trigger pulse input from the 6-pin connector on the rear panel is input through waveform shaping circuit Q8 to IC6. IC6 outputs a LAST shutter pulse and shutter OFF control pulse with the trailing edge of a pulse generated at the collector of Q8 as reference.
The LAST shutter pulse output from pin 10 of IC6 is synthesized with the XV2 pulse from IC3 using IC5.
The output period of the LAST shutter pulse is limited using a shutter OFF control pulse output from pin 6.
The resultant LAST shutter pulse is sent to IC1 as a SPECIAL shutter pulse.

d. CCD-VSUB voltage control circuit
The CCD-SUB voltage control circuit consisting of Q12, Q13, D6, D7, C1, C41, and R45 through R51 provides a proper DC voltage varying with each CCD for the overflow drain (OFD) that prevents a CCD photosensor from overflow. Adjust this circuit using RV1 while reading the value at TP1.
The reference voltage (approximately +5 V) produced from +15 V is sent to pin 3 of Q12. Pin 5 of Q12 operates so that it is parallel to this voltage. The diode at pin 1 of D60 is a clamping diode that clamps a shutter pulse into the DC voltage at TP1. The clamping diode compensates for the temperature of the diode at pin 1 using a diode at pin 2 of D6.

e. PG-BIAS voltage control circuit
The PG-BIAS voltage control circuit consisting of R54, R55, C44, and RV2 adjusts the DC bias of a PG pulse sent to the CCD. Adjust this circuit using RV2 while reading the value at TP2.

f. System clock generator
The system clock generator consists of a crystal oscillator and L-C oscillator.
Whether to select the output signal (28 MHz) of the crystal oscillator or L-C oscillator is performed automatically.
When an external sync signal (HD/VD or VS) is input from the outside of a camera, a high-level signal (+5 V) is output to pin 12 of IC1 (CXD-1084) on the SG-199 board. This control signal is sent to pin 9 of connector CN7 on the MB-403 board to control a switch circuit consisting of logic circuit IC2. The output signal of the L-C oscillator is then selected as a clock output and sent to the input pin of IC3.
The L-C oscillator constitutes some circuits on the SG-199 board and a phase-locked loop (PLL) circuit. The 28 MHz clock output from the L-C oscillator is frequency-divided using IC3 to produce a 14 MHz clock. The 14 MHz clock is sent through pin 7 of connector CN7 to the SG-199 board and input to IC1 on the SG-199 board. IC1 produces a camera's sync signal from the input clock. During external synchronization, an H SEP pulse obtained when the component of a horizontal sync signal is separated from the external sync signal is output. An H reference signal that is produced from this pulse and clock is input to phase comparator IC2 on the SG-199 board. The component of the phase difference is output from IC2.

The output phase - difference component is sent to pin 10 of connector CN7 on the MB - 403 board, passed through a low - pass filter consisting of R39, C36, and C39 on the MB - 403 board, and sent to the cathode of D5. The capacity of D5 varies depending on the voltage supplied by a variable capacitor. Therefore, the oscillation frequency of the L - C oscillator consisting of IC2, R34, L6, C29, C30, C31, C43, CT1, and D5 changes. The loop is designed to control the oscillation of a clock that determines the phase of an H reference signal so that the phase difference between the H reference signal produced from a clock and the H SEP signal separated from an external sync signal is zero ("0").

CT1 is used to suppress the partial dispersion. CT1 is set to operate in the center value (about +2.5 V cathode voltage of D5) of the PLL's variable range when the external sync signal in the center of the specification is input.

A low - level signal (0 V) is output to pin 12 of IC1 on the SG - 199 board when no external sync signal is input from the outside of a camera. For the output signal of a system clock oscillator, the output signal of a crystal oscillator is selected using a switch consisting of logic circuit IC2.

g. Clock output driver

The clock output driver consisting of Q9, Q10, Q11, R40, R41, C38, and C39 is a class B bias push - pull type cable driver. It can drive a coaxial cable with 75 ohm characteristic impedance.

The 14 MHz clock output from pin 57 of IC3 is sent through this clock output driver to pin 16 of connector CN5.

h. Video signal output driver

The video signal processed on the PR - 165 board is input from pin 6 of connector CN1 and sent to a buffer amplifier consisting of Q14, R56, and R57. The signal passed through the buffer amplifier is sent to a 14 MHz trap filter consisting of FL2, R59, and R60 to eliminate the noise of a 14 MHz component, then input to the output driver circuit.

The output driver circuit consists of Q1 through Q5, Q7, R4 through R10, R15, R16, C6, C9, and C11. It has a voltage gain that is about 1.7 times as high as usually.

A push - pull type cable driver is located as the last stage. The cable driver can drive a coaxial cable with 75 ohm characteristic impedance. The video output signal is sent through this video signal output driver to pin 9 of connector CN5.

### 2-6-5. PR-165 Board

The PR-165 board processes the video signal obtained from CCD.

a. Fixed gain amplifier
b. Black tracking pulse generator
c. Process IC
d. Sync mix circuit

a. Fixed gain amplifier

The fixed gain amplifier consisting of Q1, Q3, Q5, R10, R14 through R18, R21, R23, C8, and C10 has a voltage gain of about two times as high as usually. A CDS-processed signal from pin 6 of connector CN1 is input to the fixed gain amplifier.

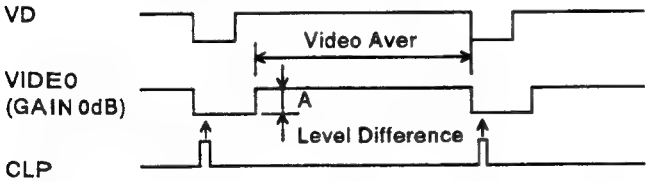
This amplifier is used to obtain a signal with high S/N ratio as the video output signal of a camera. When the GAIN mode switch on the rear panel is set to FIX, the video output signal on the RP-165 board is processed without passing through an amplifier incorporated into IC2, then output.

The gain of the amplifier incorporated into IC2 varies depending on the voltage control. The amplifier is also constituted by many transistors. Therefore, when a signal is passed through this portion, the S/N ratio of the amplifier slightly deteriorates as compared with the fixed gain amplifier above. The fixed gain amplifier is thus used to obtain a video signal with higher S/N ratio.

b. Black tracking pulse generator

The black tracking pulse generator is used to suppress the fluctuation in the black level of a video signal.

The black level of the video signal is DC-reproduced for processing using a clamp pulse. The resultant video signal is input to the processing circuit. When there is slightly a level difference between the clamp phase level and video black level, the level difference fluctuates if the gain of a video amplifier changes. Lastly, the black level fluctuates.




As shown in the figure above, if the difference between the clamp phase level and video black level is "A" when the gain is 0 dB, the level difference during 6 dB gain is 2 × A. The black level significantly floats because the clamp phase level is fixed. Therefore, analog switch IC1 is controlled using an HD signal to produce a correction pulse.

The produced correction pulse is sent to IC2 and the fixed gain amplifier and added to the video signal so that the fluctuation in the video black level using a gain disappears.

The correction pulse is produced using a circuit consisting of IC2, R4 through R9, C3, C6, C7, RV2, and RV3. The correction level for an IC2 pulse is set using RV2. The correction level for a fixed gain pulse is set using RV3.

c. Process IC

The major function of the Process IC is γ, white clip, and setup signal processing. The Process IC also outputs the video signal processed for an automatic gain control circuit and auto iris lens.

The video signal input from pin 6 of connector CN1 is input through buffer amplifier Q2 to IC2. The input signal of IC2 is first passed through an amplifier and output from IC2 once.

The amplifier in the first stage is a voltage control type of gain control amplifier. This amplifier is valid for a camera output signal when the GAIN mode switch on the rear panel is set to AUTO or MANUAL.

The CONT1 signal at pin 3 of connector CN2 is set high (+5 V) when the GAIN mode switch on the rear panel is set to AUTO or MANUAL. The output signal of analog switch IC3 then selects the output signal of gain amplifier IC2. The CONT2 signal at pin 2 of connector CN2 selects the control voltage of this gain amplifier. The output voltage of an AGC loop consisting of IC2 and external circuits (R27, R29, R33, R34, R37, R42, R43, C18, C19, C23, C25, Q7, and RV9) is selected when the GAIN mode switch is set to AUTO. The output level of a video signal is automatically kept constant for the change of incident light. The level of the video output signal is adjusted using RV9. The maximum gain is limited using RV10.

The CONT2 signal at pin 2 is set low when the GAIN mode switch is set to MANUAL. The control voltage input from pin 1 of connector CN2 is then selected as a gain amplifier control voltage. This voltage can be controlled by the volume control on the rear panel. The gain of the gain amplifier can be manually controlled by this volume control.

The video signal selected whether to be output from a fixed gain amplifier or gain amplifier IC2 is input through buffer amplifier Q10 to IC2 again.

The video signal input to IC2 is output via a γ correction circuit (GAM OUT) or output directly (LIN OUT). The GAM OUT signal is selected using switch S1 when γ is on. The LIN OUT signal is selected using switch S1 when γ is off. These signals are input through buffer amplifier Q6 to IC2 again. The video signal input to IC2 again is set up and white-clipped. The resultant video signal is output from IC2 lastly. The setup is performed using RV1 ( γ :OFF) or RV4 ( γ :ON), and the white clip is performed using RV5.

d. Sync mix circuit

The sync signal input from pin 5 of connector CN2 is level-adjusted using RV8. The adjusted sync signal is passed through buffer amplifier Q11 and mixed with a video signal. The video signal processed by IC2 is adjusted to the proper level using RV6. The adjusted video signal is sent to pin 6 of connector CN2 and output from the PR-165 board.

- In addition, a video signal for an auto iris lens is output from pin 27 of IC2. This video signal is sent through buffer amplifier Q9 to pin 4 of connector CN2 and output from the PR-165 board.

### 2-6-6. SG-199 Board

The SG-199 board is connected to an MB board via board-to-board connector. It receives the clock from the MB board, produces various sync signals from the clock, and sends it to the MB board again.

The circuits on the SG-199 board can be functionally classified into the blocks below.

a. Internal/external sync selection block
b. Sync signal generation block
c. Function set block
d. Phase comparison block

The operation for every block is described below.

a. Internal (*I) /external (*E) sync selection block

Switch S1 is used to select an internal or external sync signal output. By the setting of switch S1, +5 V is sent from the output pin of S1 as a control voltage during internal sync setting. -9 V is sent as a control voltage during external sync setting.

*1 This control voltage is input to a vertical sync signal selection circuit consisting of analog switches IC8 and IC9.

Besides, HD input/output signal is changed directly by switching S1.

* In case the board suffix -11 and -12 of SG-199 board, "EXT" and "INT" are printed on the board.

*1 [In case the board suffix -11 and -12 of SG-199 board] This control voltage is input to a horizontal sync signal selection circuit consisting of analog switches IC6 and IC7 and a vertical sync signal selection circuit consisting of analog switches IC8 and IC9.

- Internal sync signal output

*2 When switch S1 is set to "*I", +5 V is sent from the output pin of S1. Therefore, IC9 is turned on, and IC8 is turned off. The internal sync signal output mode is then selected.

The HD and VD signals output from sync signal generator IC1 are driven and HD signal is input to switch S1, also VD Signal inputs to analog switches IC9.

*2 [In case the board suffix -11 and -12 of SG-199 board] When switch S1 is set to INT, +5 V is sent from the output pin of S1. Therefore, IC7 and IC9 are turned on, and IC6 and IC8 are turned off. The internal sync signal output is then selected.

The HD and VD signals output from sync signal generator IC1 are driven and inputs to analog switches IC7 and IC9.

The drive circuit of the VD signal uses IC4.

For the HD signal, a circuit consisting of Q5, C24, R25, and R26 is used as the drive circuit so as to reduce the signal deterioration caused by the input resistance and capacity of analog switches during cable extension.

The HD and VD signals passed through analog switches are output from pins 5 and 6 of connector CN1, respectively.

Set S2 and S3 that external sync signal termination, to OFF postion for obtaining internal sync signal output.

The HD and VD signals are then passed through the MB and CN boards from the SG board and output from the connector on the rear panel to the outside of a camera.

• External sync signal input

*3 When switch S1 is set to ""E", -9 V is sent from the output pin of S1. Therefore, IC8 is turned on, and IC9 is turned off. The external sync signal input mode is then selected.
To obtain external sync operation, the two signals below can be input as an external sync signal input.
① HDI/VD signal
② VS or sync signal

*3 [In case the board suffix -11 and -12 of SG-199 board]
When switch S1 is set to EXT, -9 V is sent from the output pin of S1. Therefore, IC6 and IC8 are turned on, and IC7 and IC9 are turned off. The external sync signal input mode is then selected.

① HD/VD signal sync mode
To operate a camera in the HD/VD signal sync mode, HD and VD signals are input from the connector on the rear panel. The input enable signal levels of the HD and VD signals are 2 to 5 Vp - p. The input HD and VD signals are passed through the CN and MB boards and input from pins 5 and 6 of connector CN1.
To terminate the HD and VD signals input from the outside in 75 ohms, switches S2 and S3 for external sync signal termination are set to ON. Switch S2 corresponds to the HD signal, and switch S3 to the VD signal. To terminate no HD and VD signals in 75 ohms. S2 and S3 are set to OFF.

*4 The HD signals passed through a terminatting circuit is input to an inverter primarily consisting of Q2.

*4 [In case the board suffix -11 and -12 of SG-199 board]
The HD signals passed through a terminatting circuit is input through analog switch IC6 to an inverter primarily consisting of Q2.

In the inverter, the negative HD signal is inverted to produce a positive HD signal. The signal level then becomes approximatery 4.5 V. The resultant HD signal is passed through two-stage gate circuit IC3, waveform-shaped, and adjusted to a level of appoximatery 5 Vp-p. The signal is then sent to sync signal generator IC1 in a positive form. The gate in the second stage of gate circuit IC3 functions as aawitch.
When HD and VD signals are not input simultaneously and only the HD signal is input, the unsuitable state is detected and this gate is set to OFF. This gate functions so that the HD signal is not sent.
The VD signal is passed through a terminating circuit and input through analog switch IC8 to a sync signal separator primarily consisting of Q1 and Q3. The VD signal level becomes approximately 4 Vp - p. The resultant VD signal is passed through two - stage gate circuit IC3, waveform - shaped, and adjusted to a level of approximately 5 Vp - p. The signal is then sent to sync signal generator IC1 in a negative form.

② VS or SYNC signal sync mode
To operate a camera in the VS or SYNC signal sync mode, a VS or SYNC signal is input from the connector on the rear panel. The input enable signal level is a SYNC signal level of 0.3 Vp - p ± 6 dB. The input VS or SYNC signal is input through the CN and MB boards from pin 6 of connector CN1.
To terminate the VS or SYNC signal input from the outside in 75 ohms, switch S3 for external sync signal termination is set to ON. To terminate no VS or sync signal in 75 ohms, switch S3 is set to OFF.
The VS or SYNC signal passed through a terminating circuit is input through analog switch IC8 to a sync signal separator primarily consisting of Q1 and Q3. For the VS signal, in this sync signal separator, only a sync signal is separated from the VS signal and sent in a level of approximately 4 Vp - p. The waveform of the SYNC signal remains unchanged. The sync signal is sent in a level of approximately 4 Vp - p. This SYNC signal is passed through two - stage gate circuit IC3, waveform - shaped, and adjusted to a level of approximately 5 Vp-p. The signal is then sent to sync signal generator IC1 in a negative form.

b. Sync signal generation block
A circuit block primarily consisting of IC1 is a sync signal generator. A 14 MHz clock that the timing pulse generator on the MB board outputs is input through pin 7 of connector CN1 to IC1. IC1 produces the sync signals below required for camera operation from this clock.

| | | |
|---|---|---|
| HD | : | Horizontal sync signal |
| VD | : | Vertical sync signal |
| SYNC | : | Composite sync signal |
| BLKG | : | Blanking signal |
| FLD | : | Field identification signal |
| INT/EXT | : | Sync mode selection signal<br>Internal sync mode ····· Low<br>External sync mode ····· High |

IC1 automatically detects internal or external synchronization. If a specific signal is not input to the EXT HD pin and EXT VD pin of IC1 for more than 1024 line cycles, the internal sync mode is entered automatically.
In the normal operating mode in which no special shutter is used, therefore, the internal sync mode is entered if a signal is not input within specified period even if switch S1 is set to EXT.
The information indicating whether the camera's sync mode is internal synchronous or external synchronous is output from IC1 as a sync mode selection signal. In the internal sync mode, a low - level signal is output through pin 9 of connector CN1 from IC1 to the MB board so as to select an oscillator that generates a clock. In the external sync mode, a high - level signal is output in the same way as the above.
A spike filter consisting of D1, C4, R17, and R19 is provided in the output stage so that a BLKG signal exerts no bad influence on the definition of the video signal.

c. Function set block

Sync signal generator IC1 has various functions. These functions can be set by inputting a high- or low-level voltage to the specific input pin according to the mode to be set.

This camera has jumper lands (JR1 through JR9) for setting these functions. Each function can be set by setting the jumper lands to OPEN or SHORT according to the mode to be set.

Jumper lands JR1 through JR9 correspond to the functions below.

JR1 through JR6 : Phase advance of external horizontal sync signal

JR7 and JR8 : Restart reset/normal mode selection

JR9 : Field invert/normal mode selection

For more details of each function, refer to the corresponding item in section 2 - 5. "OPERATION MODE SETTING".

d. Phase comparsion block

A block primarily consisting of IC2 is a phase comparison block. It receives the H reference and H SEP signals output from IC1 and compares the phase. In the internal sync mode, the H SEP signal is fixed and output.

The phase comparator is then not activated. In the external sync mode, the signals below are output from IC1 as an H SEP signal as required. In the HD/VD signal sync mode, the horizontal sync signal component of an input signal is directly output. In the VS or SYNC signal sync mode, a horizontal sync component is separated from the input VS or SYNC signal in IC1. The separated signal is then output.

The H reference signal is produced from the HD signal generated in IC1. IC1 produces an HD signal from the clock signal input from the MB board. A signal whose phase is delayed relative to this HD signal proportionally to the time specified by the function setting is output to the H reference signal. Assume the phase relation between the H reference and HD signals with the HD signal as reference. The phase of the H reference signal is delayed relative to that of the HD signal by the set time. Assume the H reference signal as reference. The phase of the H reference signal is advanced relative to that of the HD signal by the set time.

As described above, the H SEP signal is produced from a horizontal sync signal input from the outside. The H reference signal is produced from an internal clock signal. To obtain proper external synchronization, the phase of a camera operation clock must coincide with that of a horizontal sync signal input from the outside. Therefore, IC2 compares the phases of the H SEP and H reference signals from IC1 and judges whether the H reference signal should be advanced or delayed to set the phase difference of these signals to zero ("0"). This result is output as a positive or negative control pulse. This control pulse is input through pin 10 of connector CN1 to the MB board, converted into a DC voltage, and input to the voltage - controlled oscillator (VCO) to control the clock frequency. The phase difference between the H SEP and H reference signals is controlled by this loop so that it is zero ("0") at all times. If the frequency deviation of a sync signal input from the outside is within ± 1 % with respect to the frequency of a reference horizontal sync signal, therefore, the camera can be operated normally.

### 2-6-7. PS-268 Board

The PS-268 board is connected to an MB board via board-to-board connector. Speaking functionally, this board is a DC power generation board. The PS-268 board supplies the DC power required for circuit operation for all the boards via the MB board.
The PS-268 board primarily consists of DC/DC converter PU1. The D/D converter is newly designed to miniaturize the XC-75/73 series and to save the power consumption. Therefore, the D/D converter is designed to satisfy the specifications (dimensions and electrical characteristics etc.) for the XC-75/73 series camera.
To normally operate D/D converter PU1, the reference input voltage of a camera supply voltage is set to Vin = 12.0 V, and the range of a guaranteed operating voltage is set to Vin = 10.5 to 15.0 V. This input supply voltage is passed through the CN and MB boards from the connector on the rear panel and input to pins 1 and 2 of connector CN1 on the PS board. When a proper supply voltage is applied to input voltage pin UNREG IN of a D/D converter, three output voltages (-9 V, +5 V, and +15 V) are obtained from the output pin. The +5 V output voltage branches into two paths on the PS board. One is sent to the dedicated analog system, and the other to the dedicated digital system. In this way, by dividing the +5 V voltage into two parts, the mutual bad influence between the 5 V lines caused by the generation of noise is prevented and the circuit malfunction and the deterioration of signal definition are suppressed. These outputs are supplied to all the boards as a DC power or reference voltage as required. The voltage value suitable for each application is used.
However, the three voltage values output from the D/D converter may be insufficient for the performance of some circuits or other voltage values may have to be supplied to some circuits. Some boards thus mount a voltage regulator circuit as required. The PS board mounts a regulator circuit primarily consisting of Q101 and Q102 that produces a -5 V voltage from the -9 V output. The regulator circuit supplies a -5 V voltage to the video signal drive circuit on the MB board. The video signal drive circuit drives the video output of a camera. The -5 V power produced on the PS board is used exclusively for the video signal drive circuit.

### 2-6-8. CN-649 Board

The CN-649 board is a sub-board mounted on the rear panel and is connected to an MB board via flexible board.
The CN-649 board mounts a 12-pin multiconnector, 6-pin connector, BNC connector, gain select switch, and manual gain volume control. The CN board primarily functions as a relay board between the external input/output connectors, gain select switch, and volume control, and the MB board.
Each operation is described below for every function.

a. Input/output connectors
CN1 is a 12-pin multiconnector. This connector has a DC IN pin. A DC power (+12 V) required for camera operation is supplied from this pin. The power input to the CN board is immediately passed through fuse F1. Consequently, this fuse is gone when abnormal power is supplied. This can prevent the main body of a camera from damage. The DC power is sent from the CN board to the PS board via the MB board, then converted into the DC power required for camera operation.
By supplying a proper power, a video output signal is sent from the MB board to the CN board. The video output signal input to the CN board is passed through a 14 MHz trap circuit to eliminate the noise of a 14 MHz component generated by a clock. The resultant signal is output from pin 4 of connector CN1 and BNC connector CN3.
CN1 has an HD signal pin (pin 6) and VD/SYNC signal pin (pin 7). The input/output setting of these pins varies depending on the sync mode.
By connecting a sync signal generator to a camera and inputting an external sync signal, the camera can be operated with external synchronization. During external synchronization, the signals shown in the table below are input from pins 6 and 7 of connector CN1 according to the desired external sync mode.

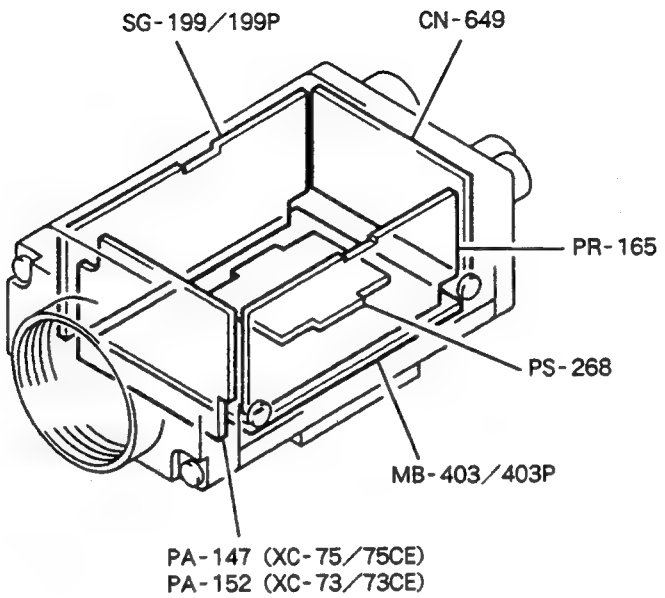
| Pin No. | External synchronization mode | | |
|---|---|---|---|
| | HD/VD | VS or SYNC | Restart / reset |
| 6 | HD signal | ——— | HD signal |
| 7 | VD signal | VS or SYNC signal | Signal reset |

During internal synchronization, HD and VD signals can be output from pins 6 and 7 of connector CN1 using a switch on the SG board.
A clock signal can be also output from CN1. Jumper land JR1 on the CN board is usually set to OPEN. A clock signal is output from pin 9 of connector CN1 by setting jumper land JR1 to SHORT. CN2 is a 6-pin connector. Generally, this connector is connected to an auto iris lens.
The video signal for the auto iris lens output from the PR board is input through the MB board to the CN board and output through a low-pass filter from pin 5 of connector CN2. The iris of the auto iris lens is automatically adjusted using this signal. The power (+12 VDC) for the auto iris lens is output from pin 6 of connector CN2.
CN2 also has the pins below for special application.
Pin 1 is a field identification signal output pin. When the camera operates in the noninterlace mode, a high-level signal is output from the SG board as a field identification signal during odd field scanning. A low-level signal is also output from the SG board during even field scanning. This signal is input from the SG board to the CN board via the MB board and output through a low-pass filter from pin 1 of connector CN2.
Pin 2 is a trigger signal input pin. To control the timing of an exposure start from the outside during special electronic shutter setting, a trigger signal is input from this pin.
For more details of the input signal condition and shutter operation, refer to the corresponding item in section 2-5. "OPERATION MODE SETTING".

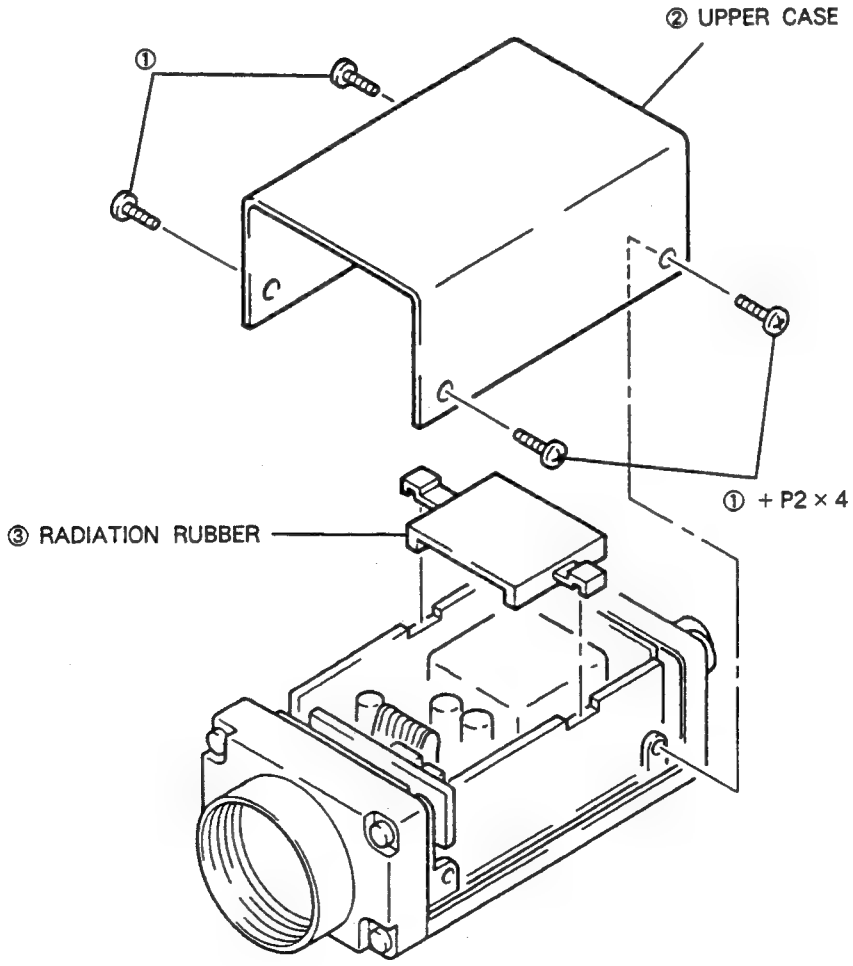
b. Gain select switch and volume control
S1 is a gain select switch. The gain of a video output signal is set using this switch.
AGC (automatic adjustment), FIX (fixed), and MANU (manual adjustment) modes are available for the gain setting. The desired mode is selected using this switch.
S1 has two output pins. A high- or low-level voltage is selected using S1 in accordance with the mode to be set and output as a control voltage. This control voltage is designed so that the combination of two output levels differs for every set mode. Therefore, the PR board that receives this voltage can judge the gain mode by the control voltage sent from the CN board via the MB board. The control voltage is input to the analog switch on the PR board as a control signal to select a switch so that the camera operates in the set gain mode.
In the MANU (manual adjustment) gain mode, the gain of the camera can be manually adjusted to the desired gain in the range of 0 dB to +18 dB using manual gain volume control RV1. The voltage value corresponding to the desired gain is output from the CN board using RV1 and sent through the MB board to the signal generator on the PR board to control the gain of a video signal amplifier.
For more details of the gain setting, refer to the corresponding item in section 2-5. "OPERATION MODE SETTING".

# SECTION 3
# SERVICE INFORMATION

## 3-1. BOARD LAYOUT

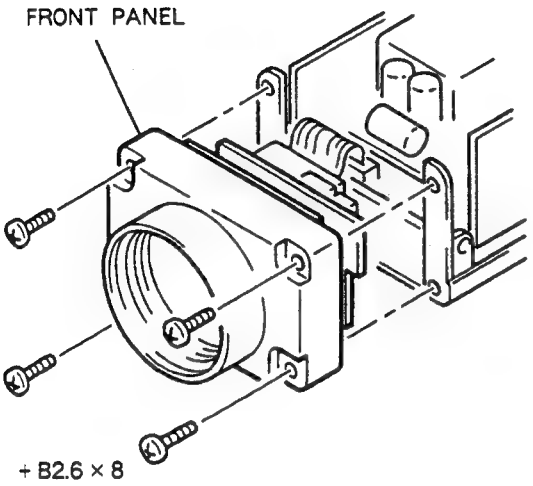



## 3-2. CABINET REMOVAL

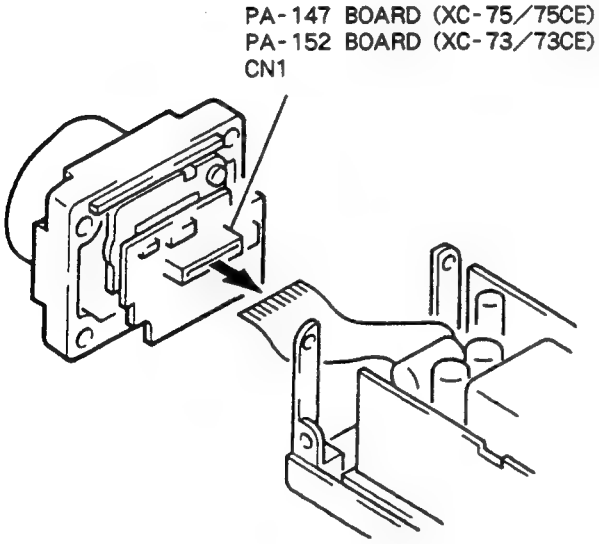


## 3-3. REPLACEMENT OF CCD UNIT

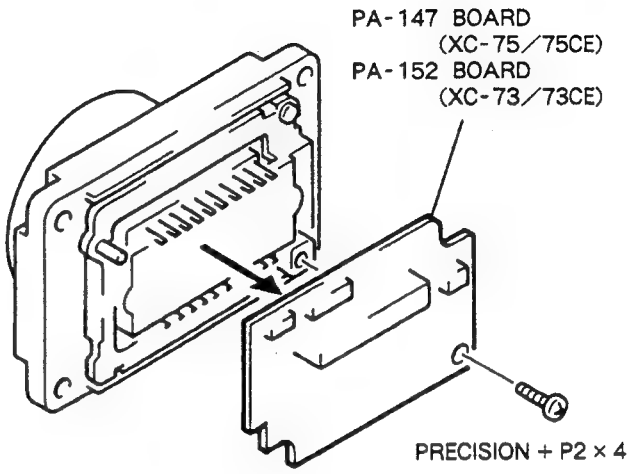
1. Remove the upper case referring to Section 3 - 2 "CABINET REMOVAL".
2. Remove the four screws (+B2.6 × 8) securing the front panel to the chassis.




3. Disconnect the connector CN1 on the PA board.




4. Remove the screw (PRECISION +P2× 4) and unsolder the PA board.

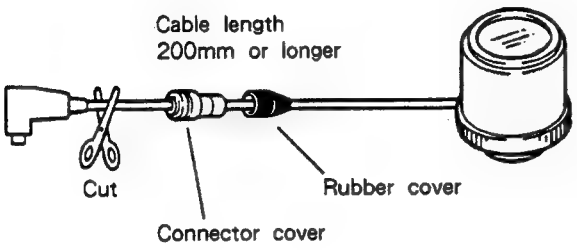



5. Replace the CCD UNIT with a new one. Assemble the unit by reversing the above procedures.
6. After the replacement of CCD UNIT is finished, be sure to perform adjustment, referring to the Section 4 "ALIGNMENT".

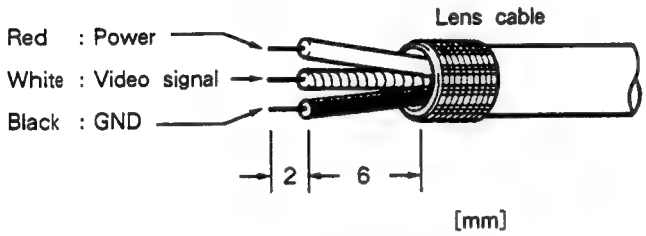
## 3-4. MODIFICATION OF AUTO-IRIS LENS

- Auto-Iris Lens: VCL-16Y
- 6-pin connector: PC-XC06

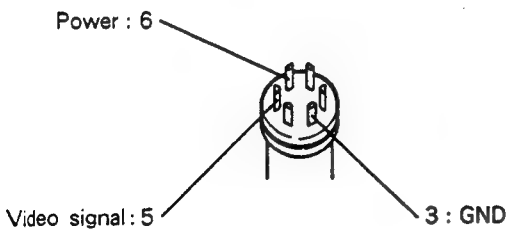
1. Cut the cable of the Auto-Iris Lens VCL-16Y so that the cable length is 200mm or longer. Thread the rubber cover and connector cover of the 6-pin connector PC-XC06 onto the cable.



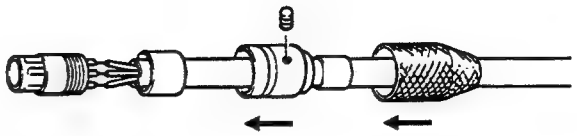

2. Perform the preparation on the inner wires of the lens cable for soldering. There are 6 inner wires (red, white and black) and cut off 3 other wires. Turn back the meshed wires.




3. Connect the 3 inner wires by soldering to the 3-pins of the 6-pin connector.

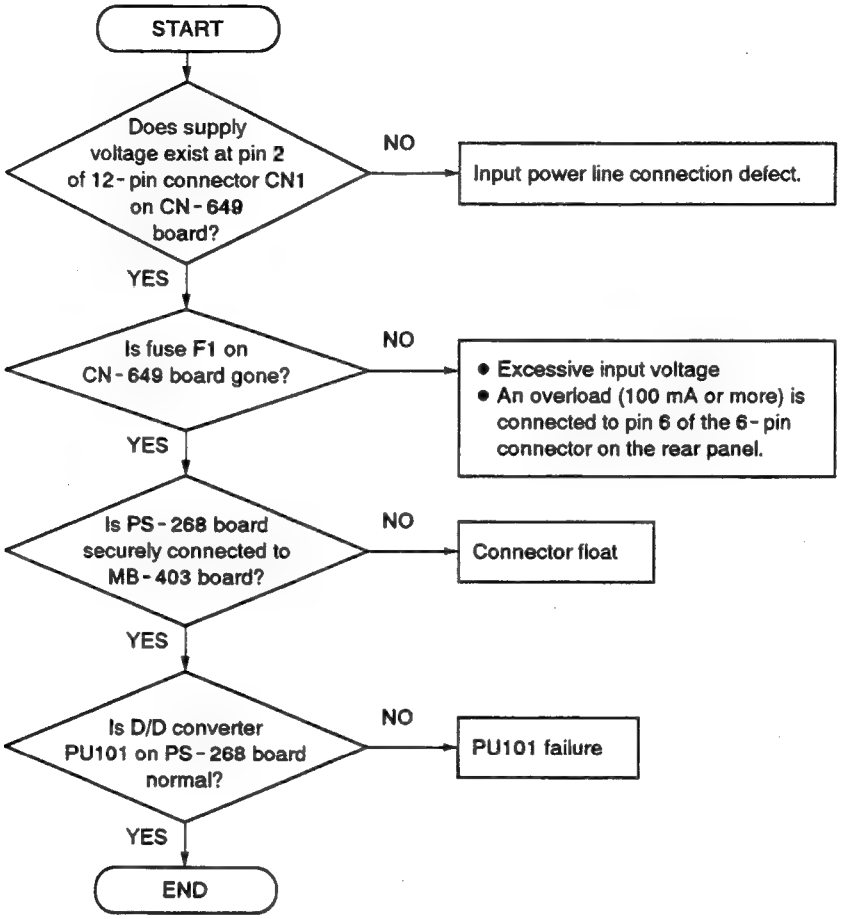



4. Wrap the turned back portion of the meshed wires with the grounding piece provided with the 6-pin connector. Slide the connector cover to cover the connected portion and fix it with the locking screw, then slide the rubber cover to cover the connector cover.

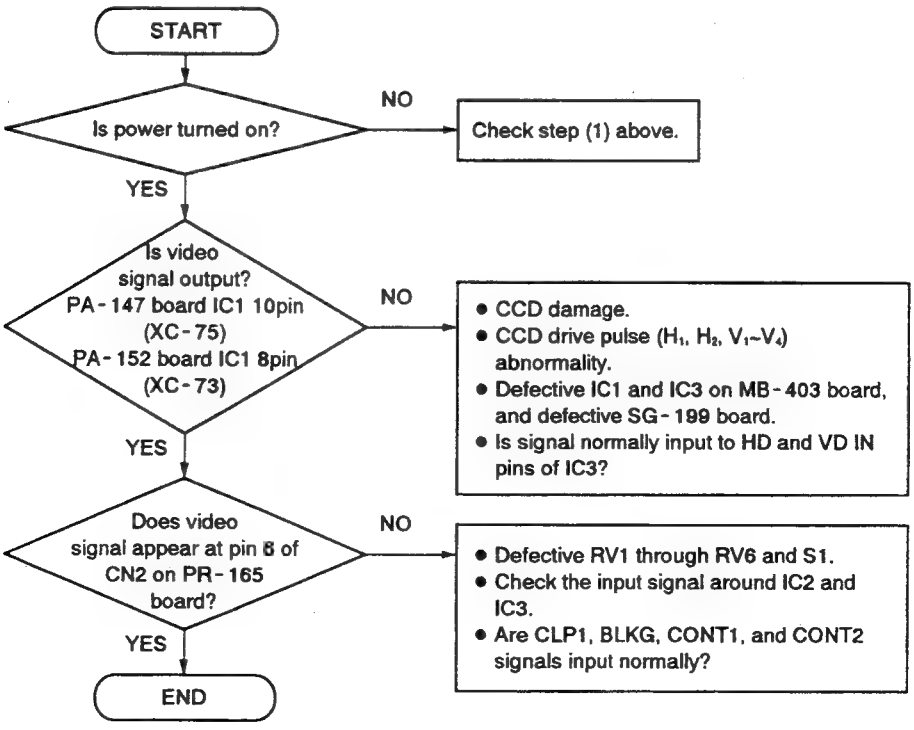


## 3-5. TROUBLESHOOTING

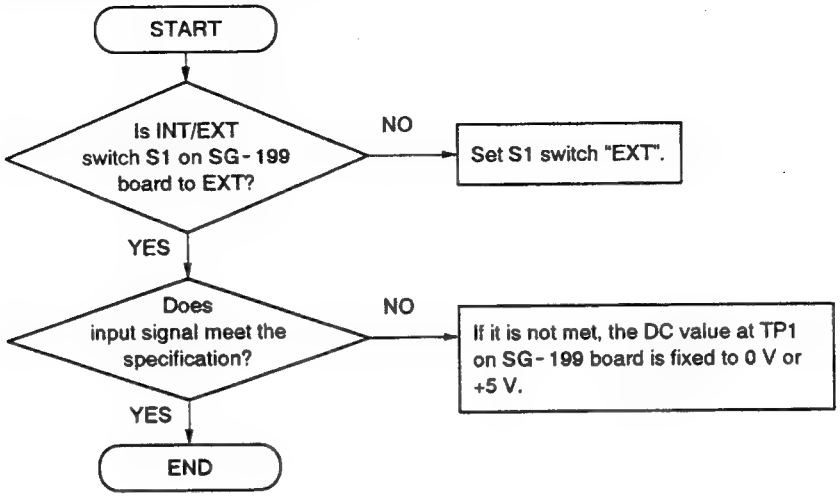
### (1) Power is not turned on.



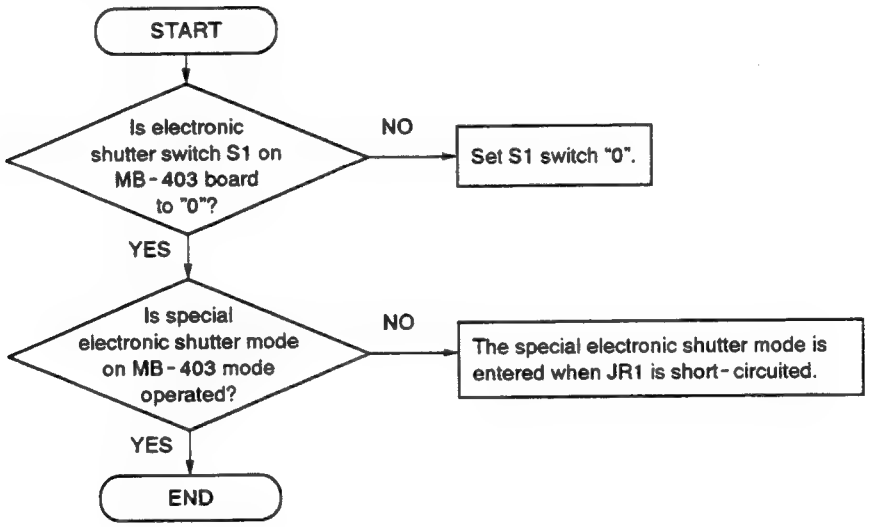

### (2) No display appears.



**(3) No external synchronization is established.**




**(4) Output display is dark excessively.**

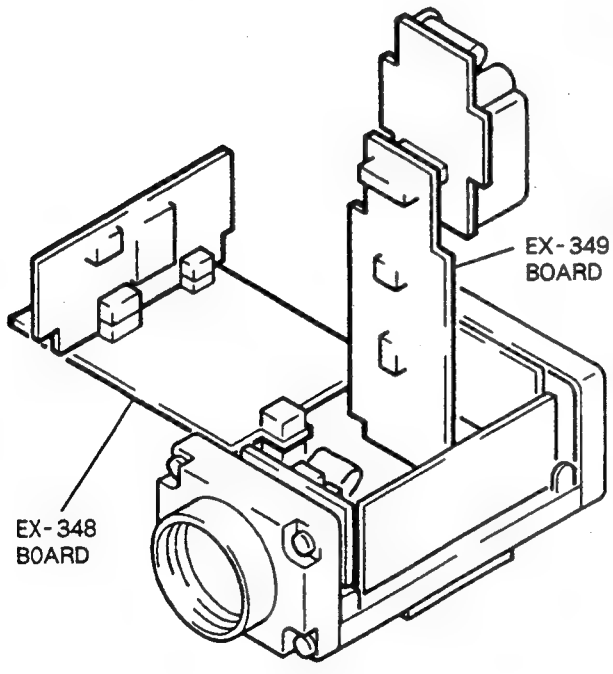


# SECTION 4
# ALIGNMENT

## 4-1. PREPARATION

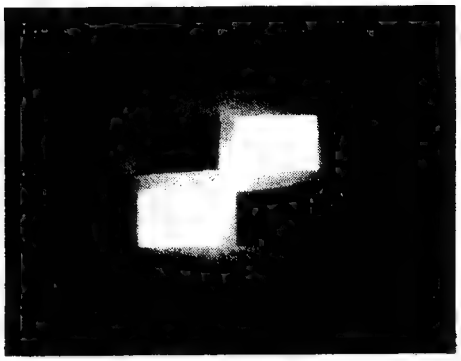
### 4-1-1. Equipment Required

- Oscilloscope
- Waveform monitor
- Black-and-white monitor
- Digital voltmeter
- Power supply unit
- Junction box JB-77(commercially available)and regulated power
- Am meter
- HD/VD signal generator(TG-7(Shibasoku))
- Frequency counter
- Tripod attachment VCT-37(Commercially available)
- Lens standard VCL-12YM
  (Commercially available)(XC-75)
  VCL-08YM
  (Commercially available)(XC-73)
- Pattern box PTB-500 or PTM-100
  Sony part No. : J-6029-140-A
- Extension board EX-348
  Sony part No. : J-6096-750-A
- Extension board EX-349
  Sony part No. : J-6096-760-A



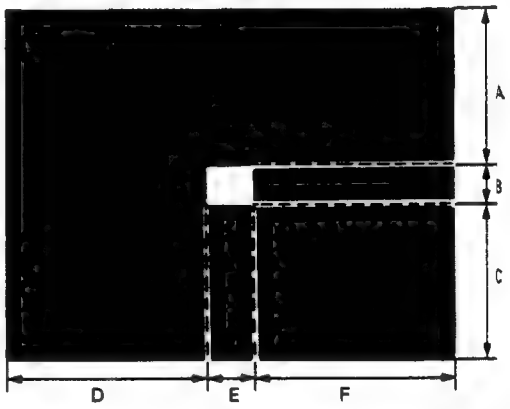

Extention of boards

- Gray scale chart
  Sony part No. : J-6026-130-A



- ND filter(50% transmittance)

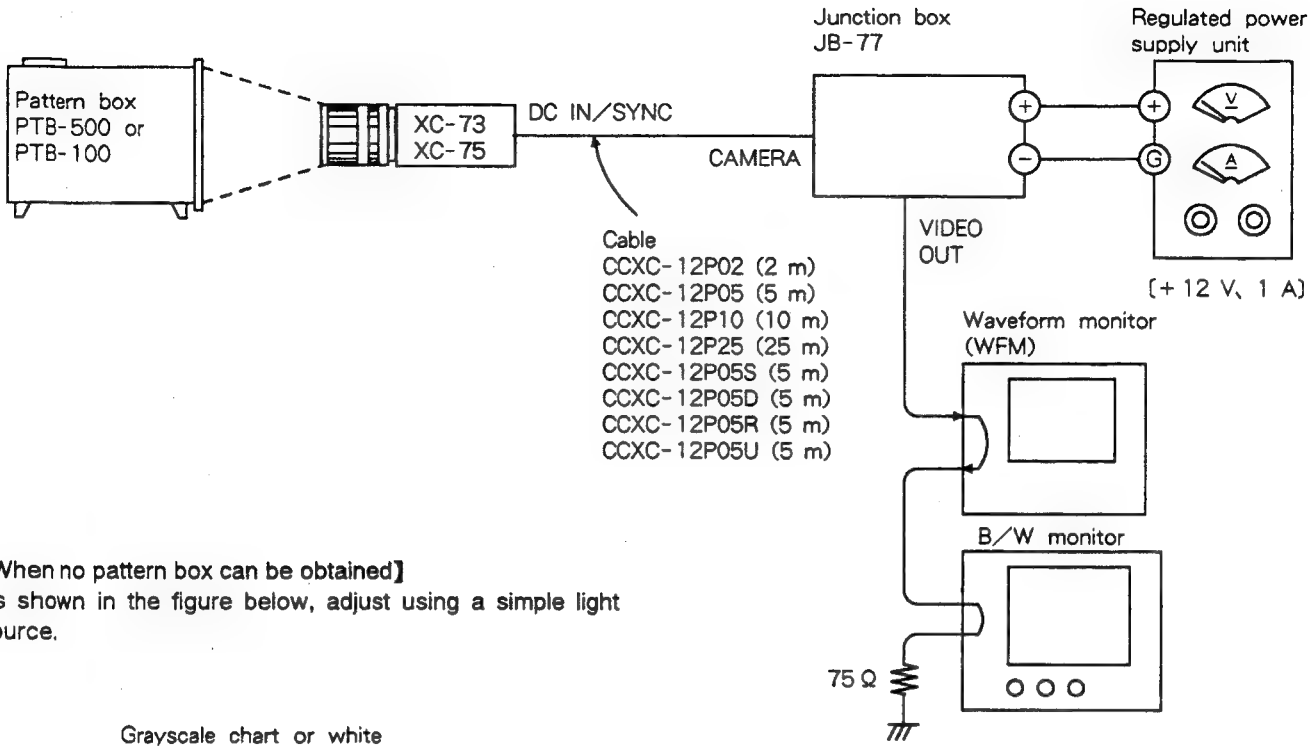
- Window chart
  Make holes on black paper as shown in the following figure. Attach an ND filter having a 10% transmittance to the window.



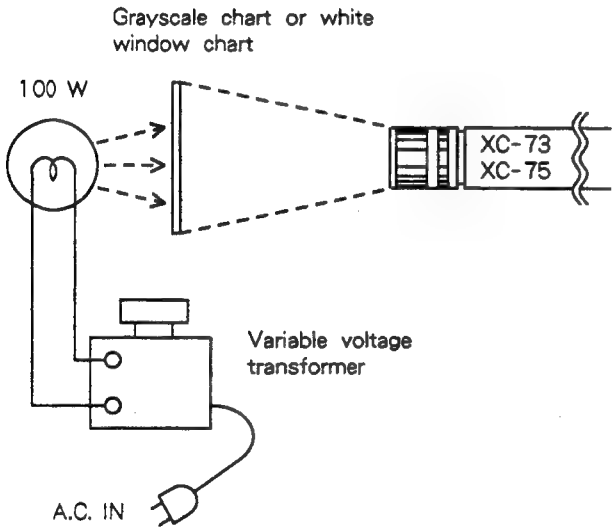

Vertical A:B:C = 4.5:1:4.5
Horizontal D:E:F = 4.5:1:4.5

【When no pattern box can be obtained】
- 100 W electric lamp
- Slidac

### 4-1-2. Connection




【When no pattern box can be obtained】
As shown in the figure below, adjust using a simple light source.




### 4-1-3. Frequency Check for Crystal Oscillator

1. Extend the SG-199 and PS-268 boards using the EX-348/349 extension boards respectively. (See Section 4-1-1. Equipment Required.)
2. Turn the power ON.
3. Connect a frequency counter to Pin 7/Extension board EX-348. Check that the specification A is met.

   A=14.31818 ± 0.001 MHz

4. If the specification is not met, replace C45 on the MB-403 board with one of the following capacitors.

| | | |
|---|---|---|
| C45 | 1pF | 1-162-905-11 |
| | 2pF | 1-162-907-11 |
| | 3pF | 1-162-908-11 |

## 4-2. OVERALL ADJUSTMENT

### Step 1. V RGL and V SUB Voltage Adjustment

**Initial setting:**

Before adjustments set the camera switches as follows.

S1/SG-199 board → EXT
S2/SG-199 board → OFF
S3/SG-199 board → OFF

**Note** : Do not perform this adjustment except when a CCD was replaced. Use a chassis for the ground of a digital voltmeter.

**Measurement equipment** : Digital voltmeter
**Measurement point** : TP1/MB-403 board
TP2/MB-403 board
**Adjustment point** : ⊘ RV1/MB-403 board
⊘ RV2/MB-403 board

**Adjustment procedure** :

1. Check the value of the label attached to the set referring to Tables 4-1 and 4-2, then check the V RGL and V SUB adjustment voltages.
2. Connect a digital voltmeter to TP1 and adjust the value to the V SUB voltage shown in Table 4-2 using ⊘ RV1 on the MB-403 board.
3. Connect a digital voltmeter to TP2 and adjust the value to the V RGL voltage shown in Table 4-1 using ⊘ RV2 on the MB-403 board.

| ① | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| Digit | 1.0 | 1.5 | 2.0 | 2.5 | 3.0 | 3.5 | 4.0 |

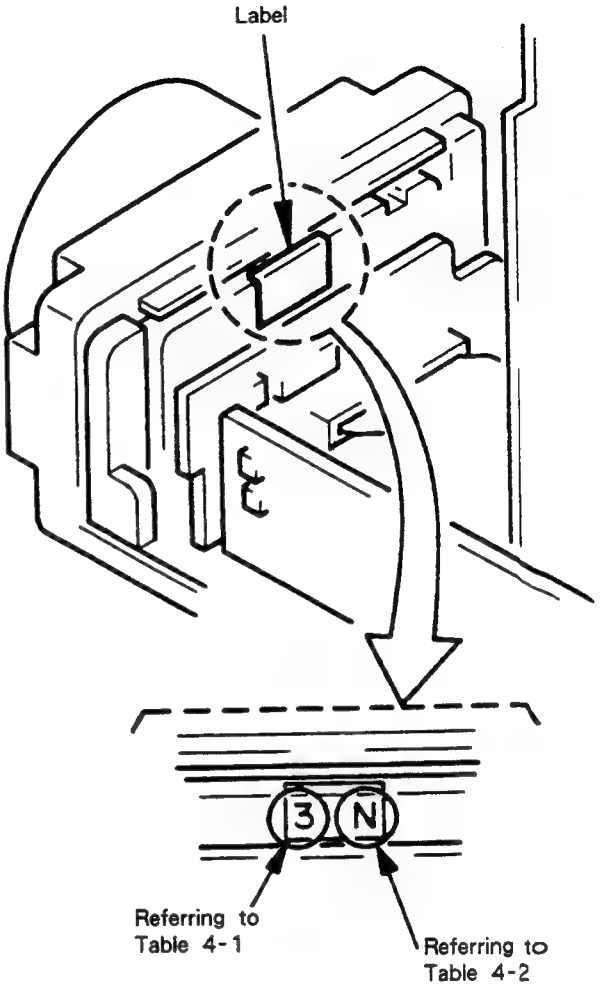
(unit:V)

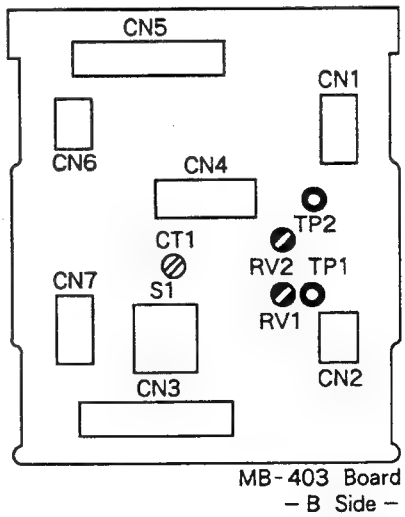
Table. 4-1.V RGL Voltage

| ② | E | f | G | h | J | K | L |
|---|---|---|---|---|---|---|---|
| Digit | 9.0 | 9.5 | 10.0 | 10.5 | 11.0 | 11.5 | 12.0 |
| ② | m | N | P | Q | R | S | T |
| Digit | 12.5 | 13.0 | 13.5 | 14.0 | 14.5 | 15.0 | 15.5 |
| ② | U | V | W | X | Y | Z | |
| Digit | 16.0 | 16.5 | 17.0 | 17.5 | 18.0 | 18.5 | |

(unit:V)

Table. 4-2.V SUB Voltage




MB-403 Board
– B Side –

### Step 2. VCO Voltage Adjustment

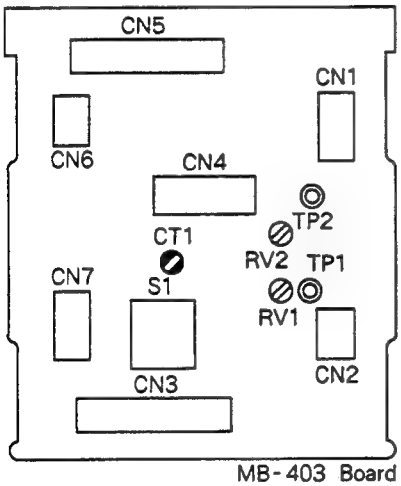
**Measurement equipment :** Digital voltmeter
**Measurement point :** TP1/SG-199 board
**Adjustment point :** ⊘ CT1/MB-403 board
**Specification :** 2.5 ± 0.1 V
**Adjustment procedure :**

1. Input a specified signal to the HD/VD input pin of junction box JB-77 using a signal generator.
2. Adjust ⊘ CT1 on the MB-403 board so that the DC level at TP1 on the SG-199 board is 2.5 ± 0.1 V.
3. Turn off the power switch, remove the extension board, and attach the PS-268 and SG-199 boards directly to the MB-403 board.
4. Turn on the power switch.

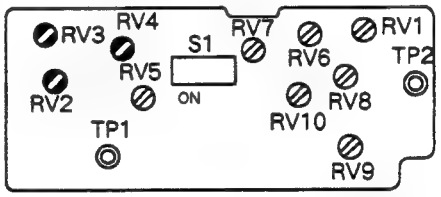
| Input Terminal | HD | VD |
|---|---|---|
| Frequency | 15.734 kHz | 525 fH/2 |

**Note :** The input levels for both VD and HD are $V_{IN}$=2.0~5.0 V p-p

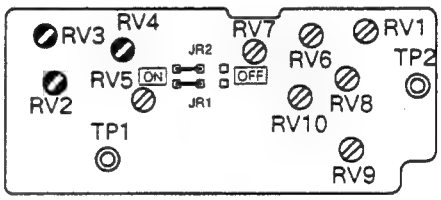
Table. 4-3



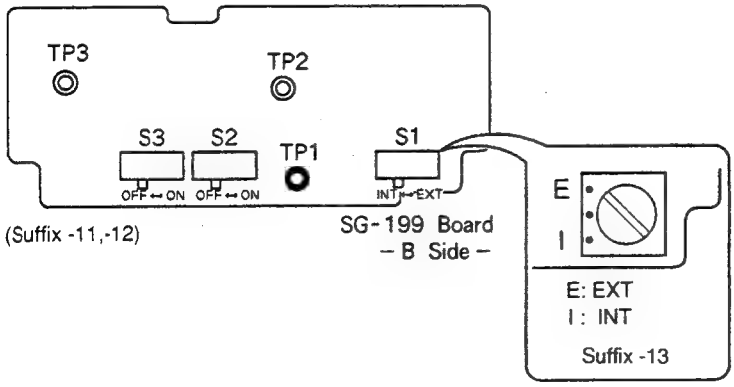

MB-403 Board
– B Side –




(Suffix -11) PR-165 Board
– B Side –




(Suffix -12) PR-165 Board
– B Side –




(Suffix -11,-12) SG-199 Board
– B Side –

### Step 3. Black Tracking Adjustment

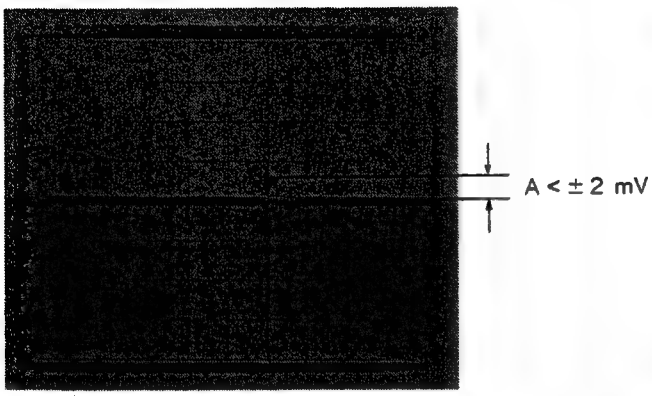
**Note :**
Perform step 3, "Black Tracking Adjustment" and step 4, "Pedestal Level Tentative Adjustment" continuously.

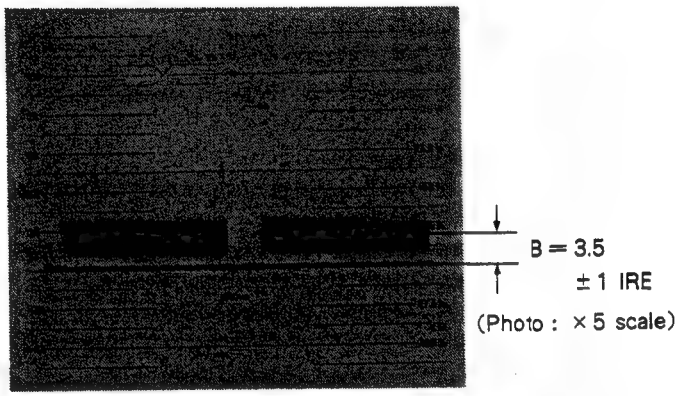
**Measurement equipment :** Oscilloscope
Waveform monitor
**Measurement point :** TP2/PR-165 board
VIDEO OUT pin/rear panel
**Adjustment point :** ⊘ RV2/PR-165 board
⊘ RV3/PR-165 board
⊘ RV4/PR-165 board
**Specification :** Level difference A < ± 2 mV
**Preparation :**

Lens → Closed
GAIN switch/rear panel → M
* S1/PR-165 board (board suffix -11) → ON
* JR1 and JR2/PR-165 board (board suffix -12) → ON
*Above settings are differ due to the board suffix number.

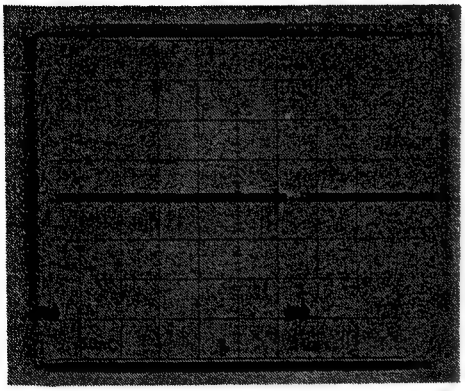
**Adjustment procedure :**

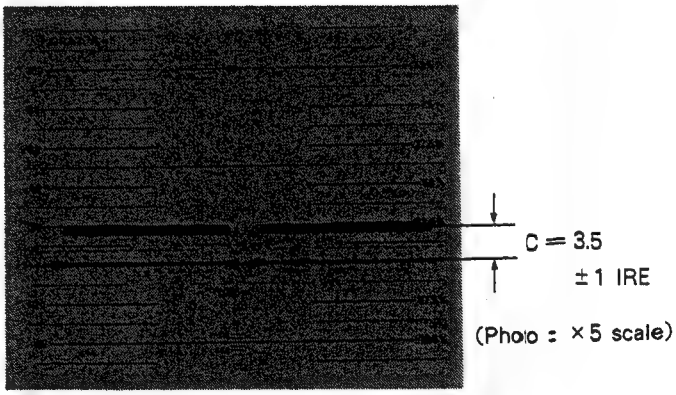
1. Turn the GAIN volume control on the rear panel fully to the right and left and check the waveform using an oscilloscope. Adjust ⊘ RV2 on the PR-165 board so that level difference A is minimum.
2. Set the GAIN switch on the rear panel to F.
3. Turn the GAIN volume control on the rear panel fully to the right and left and adjust ⊘ RV3 on the PR-165 board so that level difference A is minimum.
4. Set the GAIN switch on the rear panel to M.
5. Check the pedestal level of a VIDEO OUT signal using a waveform monitor and adjust ⊘ RV4 on the PR-165 board so that the pedestal level is 3.5 ± 1 IRE.(The change in a level is easy to read when the waveform monitor is set to SCALE × 5.)
6. Turn the GAIN volume control on the rear panel fully to the right and left and adjust ⊘ RV2 on the PR-165 board so that the fluctuation in the pedestal level of a VIDEO OUT signal is minimum.
7. Set the GAIN volume control on the rear panel to MINIMUM(turn it counterclockwise).




(GAIN : MAX)






(GAIN : MINIMUM)

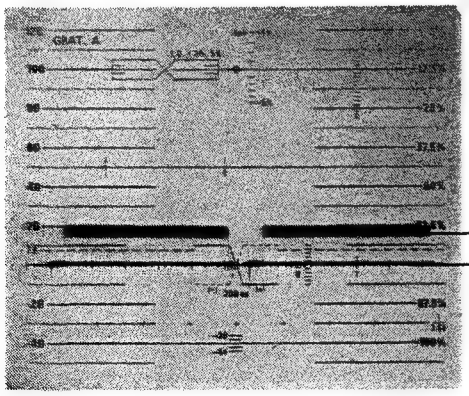
B-C : MINIMUM

### Step 4. Pedestal Tentative Adjustment

**Note :**
Perform step 3, "Black Tracking Adjustment" before performing this adjustment.

**Measurement equipment :** Waveform monitor
**Measurement point :** VIDEO OUT pin/rear panel
**Adjustment point :** ◐ RV1/PR-165 board
◐ RV3/PR-165 board
◐ RV4/PR-165 board
**Specification :** Level difference A = 3.5 ± 1 IRE
**Preparation :**
Lens → Closed
GAIN switch/rear panel → M
* S1/PR-165 board (board suffix -11) → ON
* JR1 and JR2/PR-165 board (board suffix -12) → ON
*Above settings are differ due to the board suffix number.

**Adjustment procedure :**
(The change in a level is easy to read when the waveform monitor is set to SCALE × 5.)
1. Adjust ◐ RV4 on the PR-165 board so that A = 3.5 ± 1 IRE shown in the figure below is obtained.
2. Set the GAIN switch on the rear panel to F.
3. Adjust ◐ RV3 on the PR-165 board so that A = 3.5 ± 1 IRE shown in the figure below is obtained.
4. Set the GAIN switch on the rear panel to M.
5. Set switch S1 on the PR-165 board to OFF.
6. Adjust ◐ RV1 on the PR-165 board so that A = 3.5 ± 1 IRE shown in the figure below is obtained.
7. Set the GAIN switch on the rear panel to F.
8. Using a waveform monitor, check that A = 3.5 ± 1 IRE shown in the figure below is obtained.



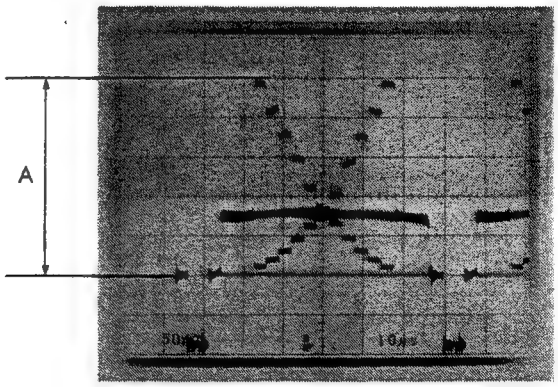
(Photo : × 5 scale)

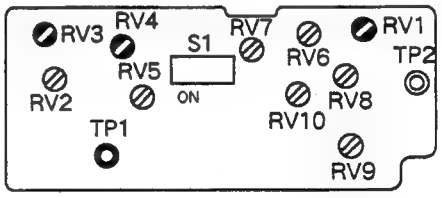
### Step 5. Reference Input Adjustment

**Measurement equipment :** Oscilloscope
**Object :** Gray scale chartt
**Measurement point :** TP1/PR-165 board
**Adjustment point :** Lens iris
**Preparation :**
* S1/PR-165 board (board suffix -11) → ON
* JR1 and JR2/PR-165 board (board suffix -12) → ON
*Above settings are differ due to the board suffix number.
(Check that ◐ RV5 is set to the position shown below.)

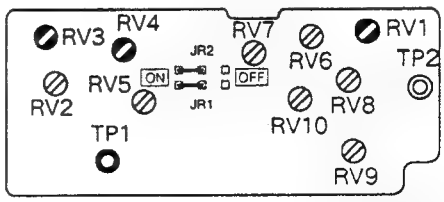

(◐ RV5 Upper side)

**Specification :** A = 250 ± 10 mV



(Suffix -11) PR-165 Board – B Side –



(Suffix -12) PR-165 Board – B Side –

### Step 6. Video Level Adjustment(1)

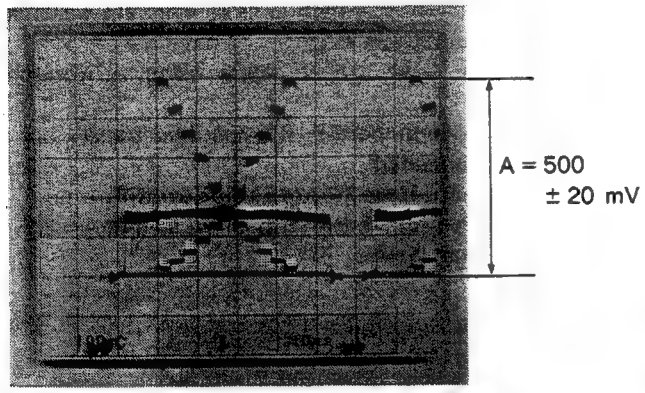
**Measurement equipment :** Oscilloscope
**Object :** Gray scale chart
**Measurement point :** TP2/PR-165 board
**Adjustment point :** ⊘ GAIN volume control/ rear panel

**Preparation :**

GAIN switch/rear panel → M
* S1/PR-165 board (board suffix -11) → ON
* JR1 and JR2/PR-165 board (board suffix -12) → ON

*Above settings are differ due to the board suffix number.

**Specification :** A = 500 ± 20 mV




### Step 7. Video Level Adjustment(2)

**Note :** Perform step 7, "Video Level Adjustment(2)" and step 8, "Sync Level Tentative Adjustment" continuously.

**Measurement equipment :** Waveform monitor
**Object :** Gray scale chart
**Measurement point :** VIDEO OUT pin/rear panel
**Adjustment point :** ⊘ RV6/PR-165 board
⊘ RV7/PR-165 board

**Preparation :**

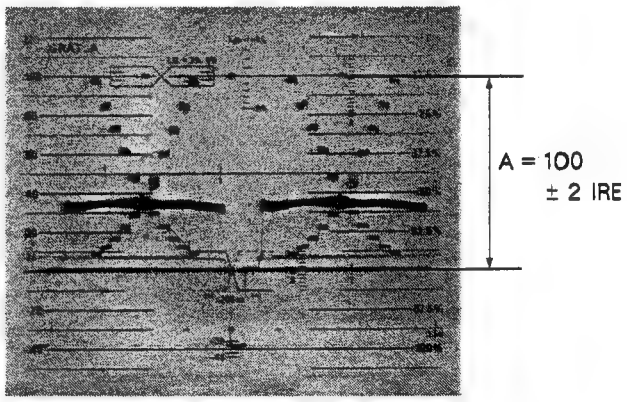
GAIN switch/rear panel → M
* S1/PR-165 board (board suffix -11) → ON
* JR1 and JR2/PR-165 board (board suffix -12) → ON

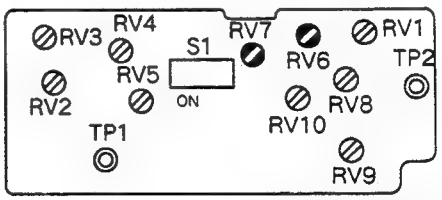
*Above settings are differ due to the board suffix number.

**Specification :** A = 100 ± 2 IRE

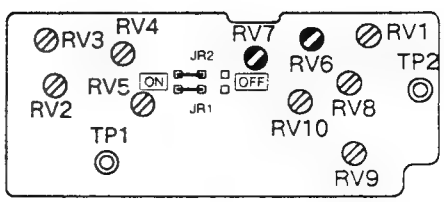
**Adjustment procedure :**

1. Adjust ⊘ RV6 on the PR-165 board so that A = 100 ± 2 IRE is obtained.
2. Set switch S1 on the PR-165 board to OFF.
3. Adjust ⊘ RV7 on the PR-165 board so that A = 100 ± 2 IRE is obtained.




(Suffix -11) PR-165 Board – B Side –




(Suffix -12) PR-165 Board – B Side –

### Step 8. Sync Level Adjustment

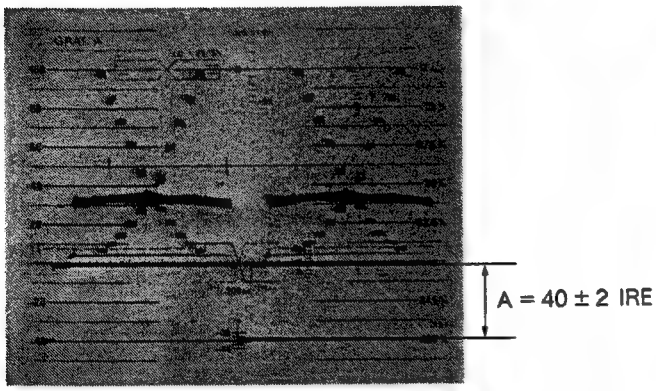
**Note** : Perform step 7, "Video Level Adjustment(2)" before performing this adjustment.
**Measurement equipment** : Waveform monitor
**Object** : Gray scale chart
**Measurement point** : VIDEO OUT pin/rear panel
**Adjustment point** : ◐ RV8/PR-165 board
**Preparation** :

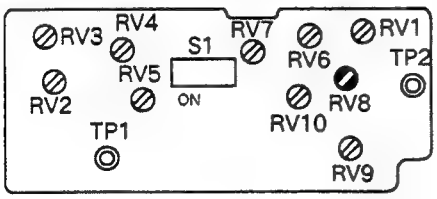
| | |
|---|---|
| GAIN switch/rear panel | → M |
| * S1/PR-165 board (board suffix -11) | → OFF |
| * JR1 and JR2/PR-165 board (board suffix -12) | → OFF |

*Above settings are differ due to the board suffix number.

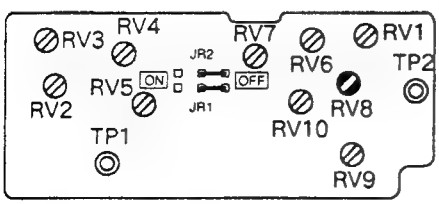
**Specification** : A = 40 ± 2 IRE

**Adjustment procedure** :
1. Check the sync signal portion of a video output signal using a waveform monitor.
2. Adjust ◐ RV8 on the PR-165 board so that A = 40 ± 2 IRE is obtained.
3. Perform step 7, "Video Level Adjustment(2)" once again after this adjustment.




(Suffix -11) PR-165 Board – B Side –




(Suffix -12) PR-165 Board – B Side –

### Step 9. Pedestal Adjustment

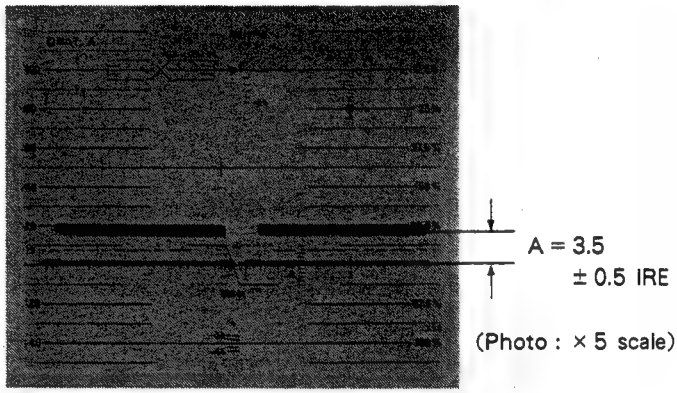
**Measurement equipment** : Waveform monitor
**Measurement point** : VIDEO OUT pin/rear panel
**Adjustment point** : ◐ RV4/PR-165 board
◐ RV1/PR-165 board
**Preparation** :

| | |
|---|---|
| Lens | → Closed |
| GAIN switch/rear panel | → F |
| * S1/PR-165 board (board suffix -11) | → ON |
| * JR1 and JR2/PR-165 board (board suffix -12) | → ON |

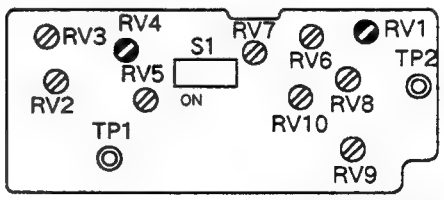
*Above settings are differ due to the board suffix number.

**Specification** : A = 3.5 ± 0.5 IRE

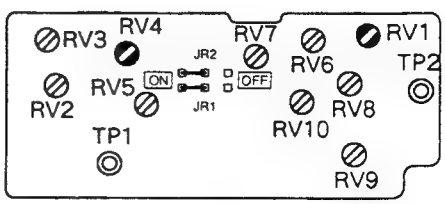
**Adjustment procedure** :
(The change in a level is easy to read when the waveform monitor is set to SCALE × 5.)
1. Check the video output signal using a waveform monitor.
2. Adjust ◐ RV4 on the PR-165 board so that A = 3.5 ± 0.5 IRE is obtained.
3. Set switch S1 on the PR-165 board to OFF.
4. Adjust ◐ RV1 on the PR-165 board so that A = 3.5 ± 0.5 IRE is obtained.




(Photo : × 5 scale)




(Suffix -11) PR-165 Board – B Side –




(Suffix -12) PR-165 Board – B Side –

### Step 10. White Clip Adjustment

**Measurement equipment :** Waveform monitor
**Measurement point :** VIDEO OUT pin/rear panel
**Adjustment point :** ◐ RV5/PR-165 board
**Preparation :**

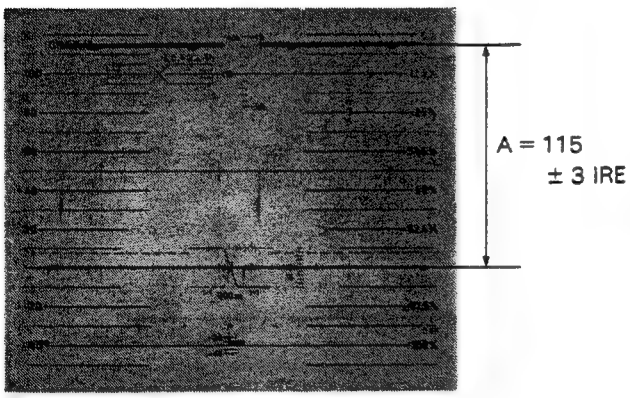
| | |
|---|---|
| Lens | → Open |
| GAIN switch/rear panel | → F |
| * S1/PR-165 board (board suffix -11) | → OFF |
| * JR1 and JR2/PR-165 board (board suffix -12) | → OFF |

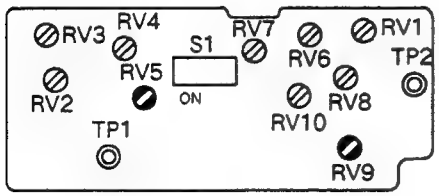
*Above settings are differ due to the board suffix number.

**Specification :** A = 115 ± 3 IRE

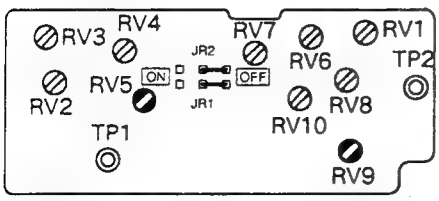
**Adjustment procedure :**

1. Check the video output signal using a waveform monitor.
2. Adjust ◐ RV5 on the PR-165 board so that A = 115 ± 3 IRE is obtained.




(Suffix -11) PR-165 Board – B Side –




(Suffix -12) PR-165 Board – B Side –

### Step 11. Automatic Gain Control(AGC)Adjustment

**Measurement equipment :** Oscilloscope
Waveform monitor
**Object :** Gray scale chart (ND filter)
**Measurement point :** VIDEO OUT pin/rear panel
**Adjustment point :** ◐ RV9/PR-165 board
**Preparation :**

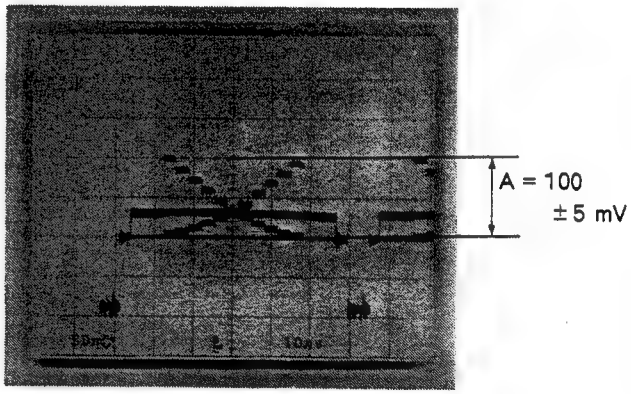
| | |
|---|---|
| GAIN switch/rear panel | → F |
| * S1/PR-165 board (board suffix -11) | → OFF |
| * JR1 and JR2/PR-165 board (board suffix -12) | → OFF |

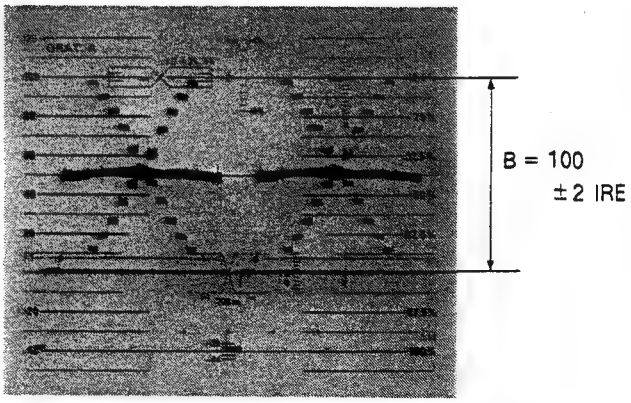
*Above settings are differ due to the board suffix number.

**Specification :** A = 100 ± 5 mV
B = 100 ± 2 IRE

**Adjustment procedure :**

1. Install the ND filter (50% transmittance) on the lens.
2. Shoot a gray scale chart and check the waveform at TP1 on the PR-165 board.
3. Adjust the lens iris so that A = 100 ± 5 mV is obtained.
4. Check the video output signal using a waveform monitor.
5. Set the GAIN switch on the rear panel to A.
6. Set switch S1 on the PR-165 board to ON.
7. Adjust ◐ RV9 on the PR-165 board so that B = 100 ± 2 IRE is obtained.



### Step 12. Maximum Gain Adjustment

**Measurement equipment :** Oscilloscope
Waveform monitor
**Object :** Window chart
**Measurement point :** VIDEO OUT pin/rear panel
**Adjustment point :** ⊘ RV10/PR-165 board
**Preparation :**

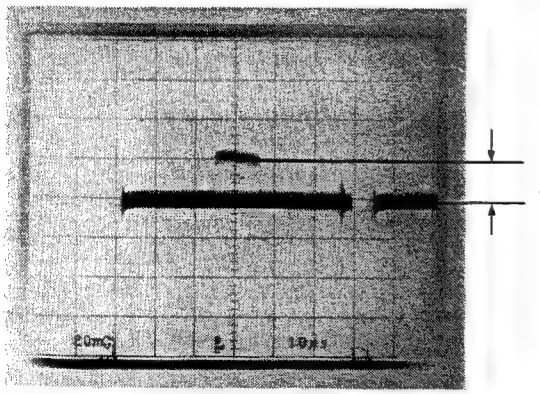
GAIN switch/rear panel → A
* S1/PR-165 board (board suffix -11) → OFF
* JR1 and JR2/PR-165 board (board suffix -12) → OFF

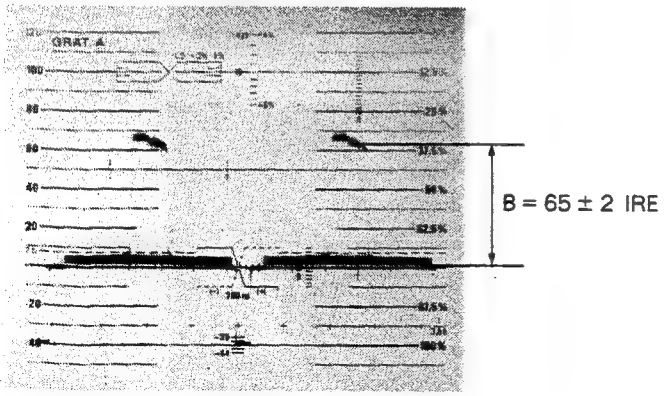
*Above settings are differ due to the board suffix number.

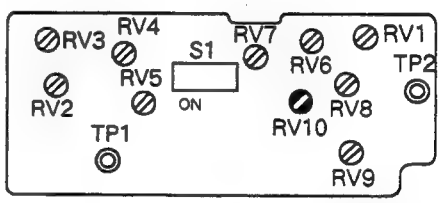
**Specification :** B = 65 ± 2 IRE

**Adjustment procedure :**

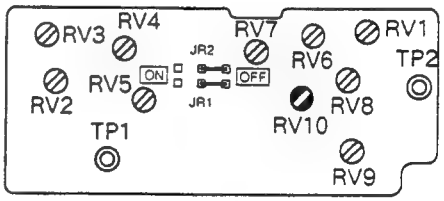
1. Shoot a window chart and check the waveform at TP1 on the PR-165 board.
2. Adjust the lens iris so that A = 20 ± 1 mV is obtained.
3. Check the video output signal using a waveform monitor.
4. Adjust ⊘ RV10 on the PR-165 board so that B = 65 ± 2 IRE is obtained.




(Suffix -11) PR-165 Board – B Side –




(Suffix -12) PR-165 Board – B Side –

**Note :**

- Set *JR1 and *JR2 on the PR-165 board to ON or OFF position according to user request.
  *In case of board suffix -11, S1 switch is available instead of JR1 and JR2.
- After adjustment is completed, set the camera switches as follows.

  S2/SG-199 board → ON
  S3/SG-199 board → ON
  GAIN switch/rear panel → F

# SECTION 2
# COMPREHENSIVE SPECIFICATIONS

## 2-1. SPECIFICATIONS(XC-73CE/75CE)

### Imaging system

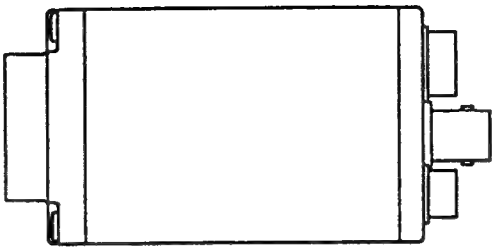
| | |
|---|---|
| Pickup device | Interline-transfer CCD |
| Effective picture elements | 752 × 582 (horizontal/vertical) |
| Sensing area | XC-73CE: 1/3-inch size<br>XC-75CE: 1/2-inch size |
| Optical blank | 43 elements on each horizontal line. |
| CCD vertical drive frequency | 15.625 kHz ± 1% |
| CCD horizontal drive frequency | 14.1875 MHz |
| Signal system | CCIR system |
| Cell size | XC-73CE: 6.5 × 6.25 μ m (horizontal/vertical)<br>XC-75CE: 8.6 × 8.3 μ m (horizontal/vertical) |

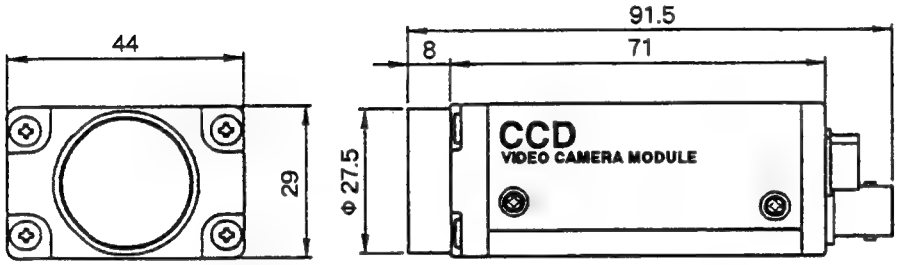
### Optical system and others

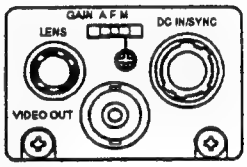
| | |
|---|---|
| Lens mount | C mount |
| Flunge focal length | 17.526 mm |
| Synchronization | Internal/external (automatically switched according to input signal) |
| External sync signal | S, VS (sync level: $0.3^{+0.3}_{-0.15}$ Vp-p) |
| I/O | HD/VD (HD/VD level: 2-5 Vp-p, automatically switched between HD/VD according to input signal, and I/O selection by internal switch) |
| External sync allowable frequency | ± 1% (of horizontal sync frequency) |
| Jitter | Within ± 50 nsec |
| Scanning system | 625 lines<br>2:1 interlace/noninterlace (automatically switched according to input signal) |
| Video output | 1.0 Vp-p, sync negative, 75 ohms unbalanced |
| Horizontal resolution (When using VCL-08 YM lens with any iris adjustment from "open" to F11) | 560 TV lines |
| Vertical effective lines | 575 lines (with 2:1 interlace) |
| Sensitivity | 400 lux, F4 ( γ compensation ON, 0 dB) |
| Minimum illumination | 3.0 lux (AGC mode, F1.4, γ compensation ON) |
| Video S/N ratio | 54 dB |
| Gain | AGC/Fixed gain/Manual gain control (selected by switch on the rear panel) |
| γ | γ compensation/ γ =1<br>* (selected by internal jumpers)<br>* The internal switch is mounted instead of internal jumpers in the following serial number for the camera module.<br>Serial number ;<br>XC-73CE (EK) : 400001 - 405150<br>XC-75CE (EK) : 10001 - 53000 |
| White clip | 115 ± 10 % |
| Charge accumulation | Frame/Field (switched by internal jumper change) |
| Shutter | Normal shutter/Special shutter (switched by internal jumper change) |
| Shutter speed | Normal shutter: Flickerless 1/125, 1/250, 1/500, 1/1000, 1/2000, 1/10000 sec. (selected by internal switch)<br>Special shutter: 1/1500 to 1/80 sec. |
| Power | +12 V DC (Range: 10.5 to 15 V) |
| Power consumption | XC-73CE: 1.4 W<br>XC-75CE: 1.6 W |
| Temperature | Operating: -5 to +45 °C (41 to 113 °F)<br>Storage: -25 to +60 °C ) (77 to 140 °F) |
| Relative humidity | Operating: 20 to 80 %<br>Storage: 20 to 95 % |
| Vibration resistance | 7 G (11 Hz-200 Hz) |
| Shock resistance | 70 G |
| External dimension (w/h/d) | 44 × 29 × 91.5 mm (1 3/4 × 1 3/6 × 3 5/8 inches) (including external projection) |
| Mass | 140 g (5 oz) |
| Accessories | Lens mount cap (1)<br>Operation manual (1) |

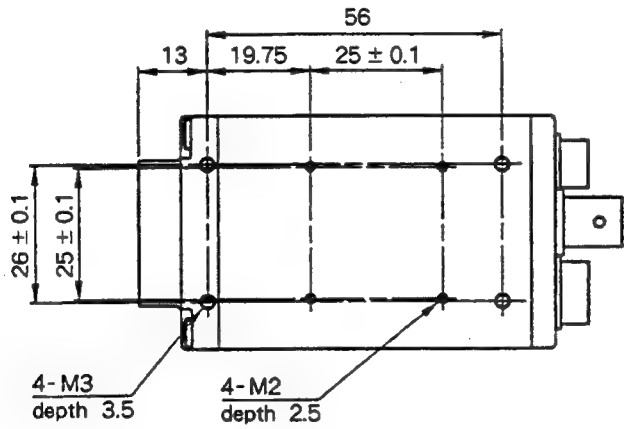
Design and specifications are subject to change without notice.

**Dimensions:**
**Camera Module <XC-75CE>**

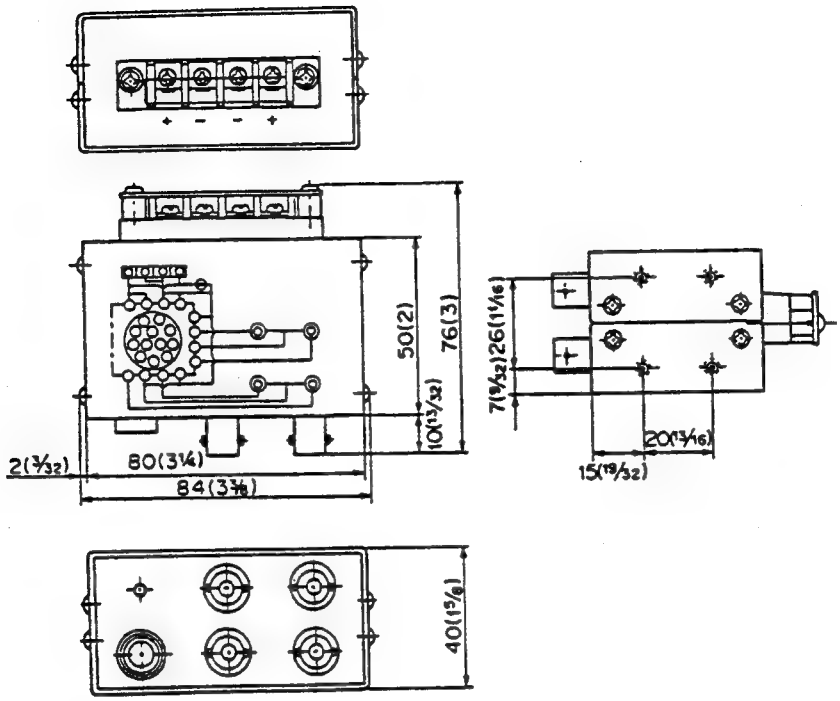




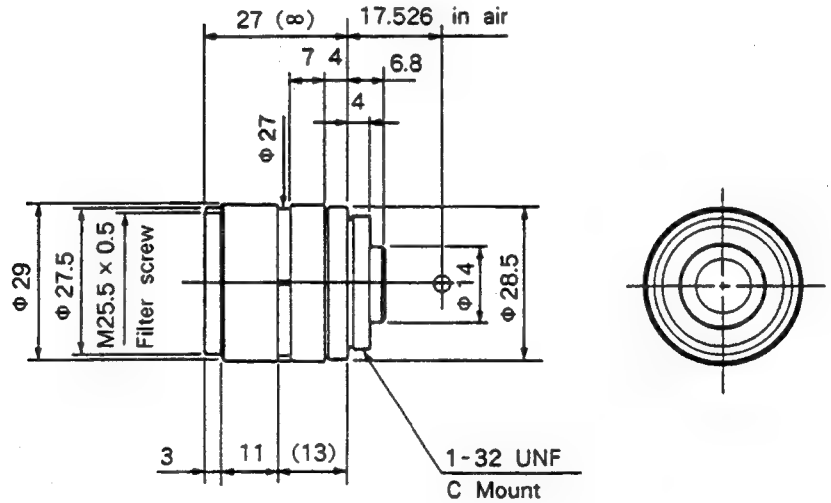



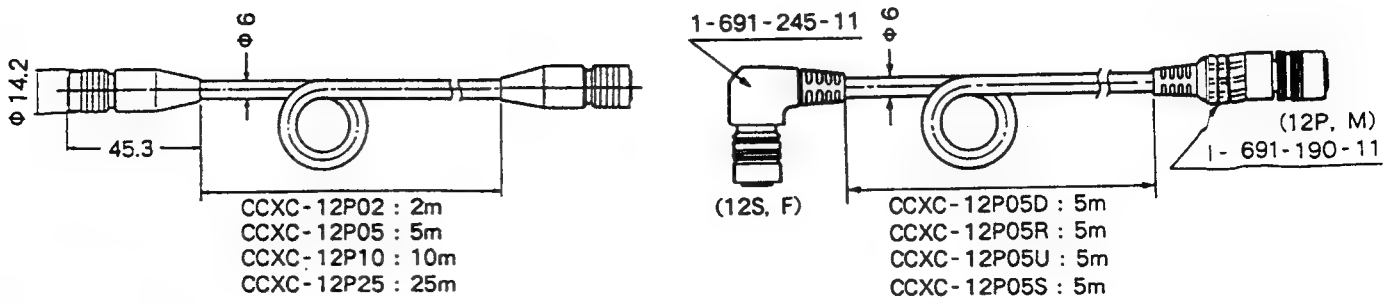
**Junction box**




**Lens**

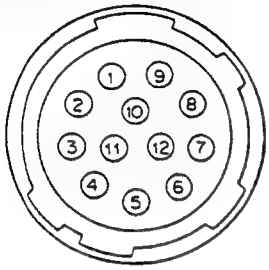



**Camera cable**



## 2-2. CONNECTORS PIN FUNCTION

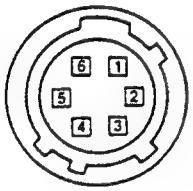
### 12P Multiconnector (External view)




| PIN No. | EXTERNAL SYNC MODE | | | CAMERA SYNCRONOUS OUTPUT |
|---|---|---|---|---|
| | HD/VD | VS | RESTART RESET | |
| 1 | GND | GND | GND | GND |
| 2 | DC+12V | DC+12V | DC+12V | DC+12V |
| 3 | VIDEO OUTPUT (GND) | VIDEO OUTPUT (GND) | VIDEO OUTPUT (GND) | VIDEO OUTPUT (GND) |
| 4 | VIDEO OUTPUT (SIGNAL) | VIDEO OUTPUT (SIGNAL) | VIDEO OUTPUT (SIGNAL) | VIDEO OUTPUT (SIGNAL) |
| 5 | HD INPUT (GND) | — | HD INPUT (GND) | HD OUTPUT (GND) |
| 6 | HD INPUT (SIGNAL) | — | HD INPUT (SIGNAL) | HD OUTPUT (SIGNAL) |
| 7 | VD INPUT (SIGNAL) | VS INPUT (SIGNAL) | RESET PULSE (SIGNAL) | VD OUTPUT (SIGNAL) |
| 8 | — | — | — | CLOCK OUTPUT (GND) |
| 9 | — | — | — | CLOCK OUTPUT (SIGNAL) |
| 10 | GND | GND | GND | GND |
| 11 | DC+12V | DC+12V | DC+12V | DC+12V |
| 12 | VD INPUT (GND) | VS INPUT (GND) | RESET PULSE (GND) | VD OUTPUT (GND) |

NOTE HD/VD input level ; 2-5Vp-p, negative *
VS SYNC level ; 0.3-1.2Vp-p, negative *
* Either 75- Ω termination input or high impedance input is selectable using S2/SG-199P Board

### 6P Lens Connector (External view)

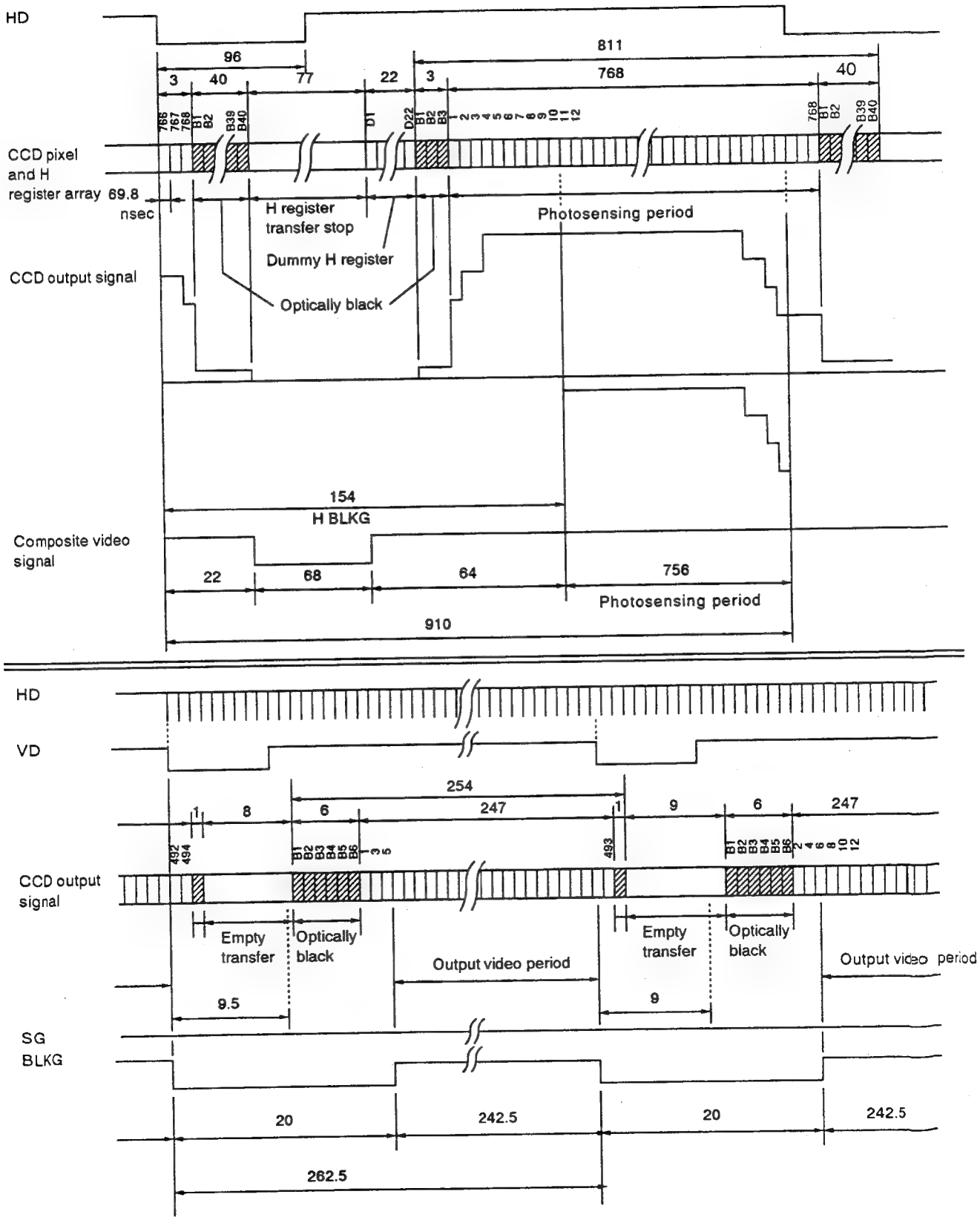



| PIN No. | SIGNAL | SPECIFICATION |
|---|---|---|
| 1 | FLD OUT | FLD IN |
| 2 | TRIGGER | TRRIGER |
| 3 | GND | GND |
| 4 | NC | NC |
| 5 | VS OUT | VIDEO SIGNAL OUTPUT |
| 6 | +12 OUT | DC+12V OUT |

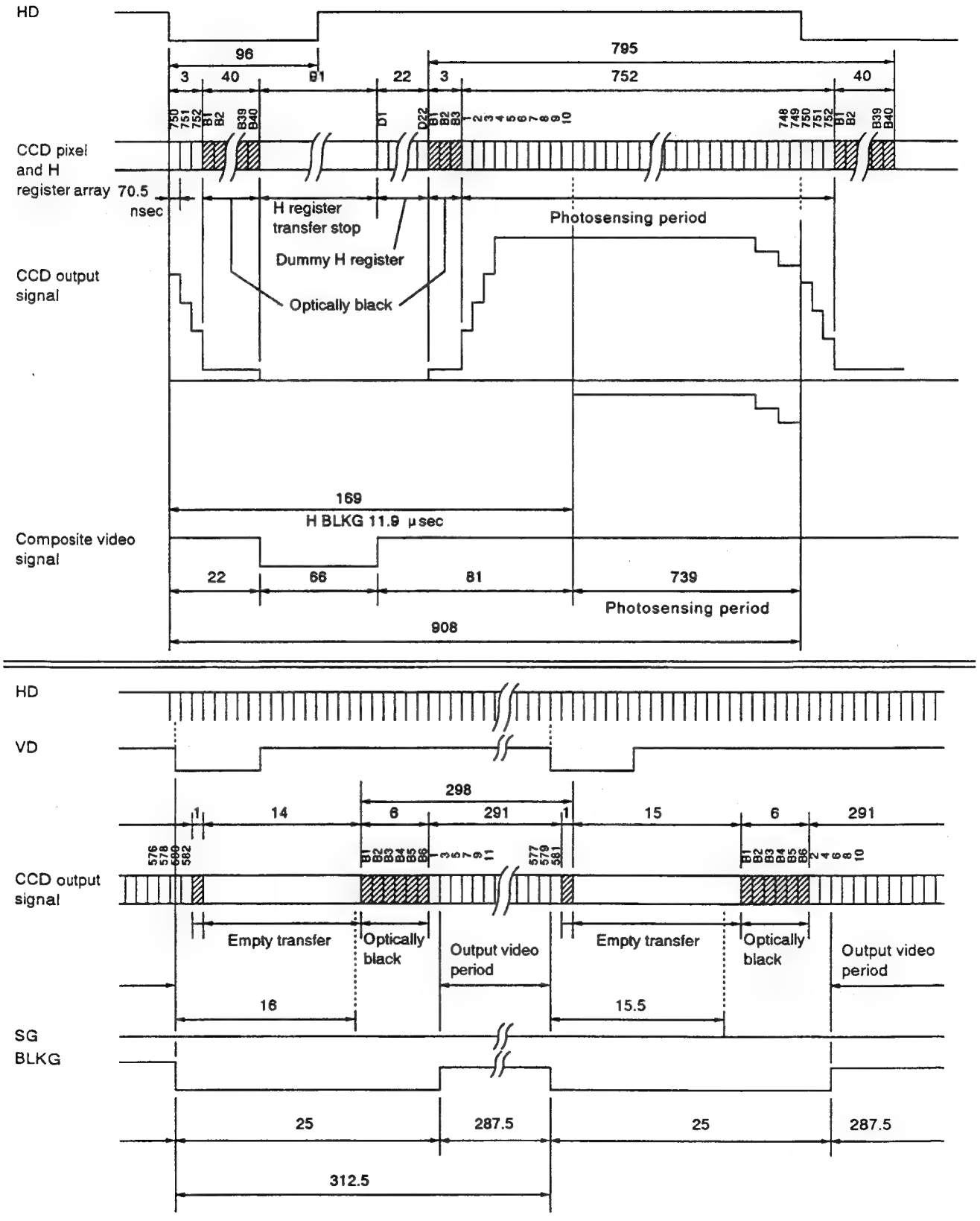
Note)
The video signal at pin ⑤ is for the AUTO-IRIS lens, so it cannot be terminated by 75 Ω.

## 2-3. TIMING CHART OF CCD OUTPUT WAVEFORMS

### 2-3-1. EIA



## 2-3-2. CCIR


HD
96
795
3
40
B1
22
3
752
40
CCD pixel and H register array
70.5 nsec
H register transfer stop
Dummy H register
Optically black
Photosensing period
CCD output signal
169
H BLKG 11.9 µsec
Composite video signal
22
66
81
739
Photosensing period
908
HD
VD
298
1
14
6
291
1
15
6
291
CCD output signal
Empty transfer
Optically black
Output video period
Empty transfer
Optically black
Output video period
16
15.5
SG
BLKG
25
287.5
25
287.5
312.5

## 2-4. EXTERNAL SYNCHRONIZATION

There are three external synchronization modes:
1. VS/VBS mode
2. HD and VD mode
3. RESTART RESET mode

### 2-4-1. VS/VBS Mode

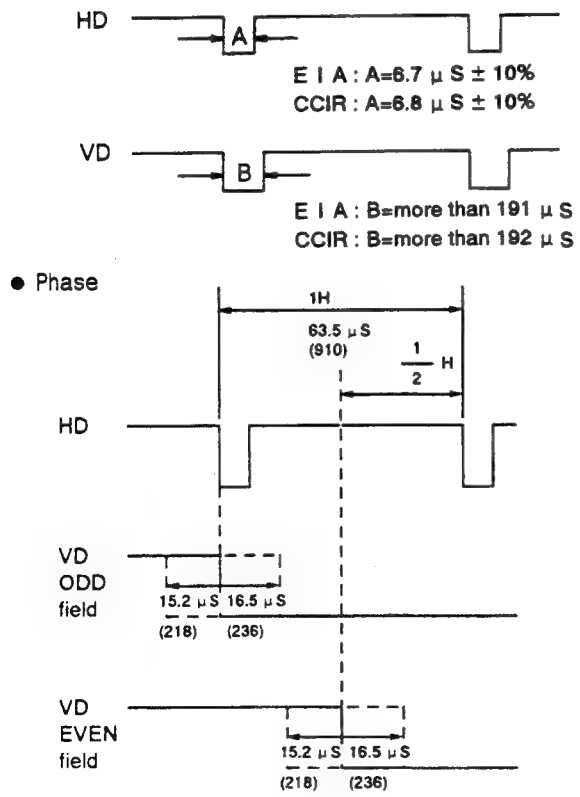
The VS/VBS mode provides external synchronization by supplying a normal composite signal, VS or VBS, to pin 7 of the 12-pin connector.

### 2-4-2. HD and VD Mode

The HD and VD mode provides external synchronization by supplying an HD signal to pin 6 and a VD signal to pin 7 of the 12-pin connector.

**Input conditions of HD and VD signals**

- Frequency (period)
  HD : 15.625 kHz ± 1%(64 μs ± 1%)
  VD : 294 to 1023 1/2 H
  *The maximum number of vertical effective lines is 581 in the interlace mode.
  In the non-interlace mode, it is 290 for both the ODD field and the EVEN field.




The figure in parentheses ( ) indicates the number of clock pulses

As shown in the illustration above, the ODD field is provided when the phase shift between the trailing edge of the VD signal and the trailing edge of the HD signal is between a lead of 15.1 μs and a lag of 16.5 μs. The EVEN field is provided when the phase shift between the trailing edge of the VD signal and the point 1/2H from the trailing edge of the HD signal is between a lead of 15.1 μs and a lag of 16.5 μs.

**Interlace and non-interlace**

Operation can be preformed in either interlace or non-interlace mode by changing the input condition of the VD signal. See Figure 1.

- Interlace
  To operate in the interlace mode, set the period of the VD signal to (A + 1/2)H. A is an integer, 294 to 1023. In other words, the phase of the leading edge of the VD signal against the leading edge of the HD signals is changed for each VD signal. The field changes from ODD to EVEN and to ODD, repeatedly during operation in the interlace mode. At this time, the number of scanning lines per frames is 2A + 1.

- Non-interlace
  To operate in the non-interlace mode, set the period of the VD signal to A H. A is an integer, 294 to 1023. In other words, the phase of the leading edge of the VD signal against the leading edge of the HD signal is not changed for each VD signal, and the field ODD or EVEN remains unchanged for operation in the non-interlace mode. The number of scanning lines is A; this is half of the number of scanning lines for operation in the interlace mode. The sensitivity is half of the sensitivity provided in the interlace mode, when the frame is stored. See Figure 2.

### 2-4-3. RESTART RESET Mode

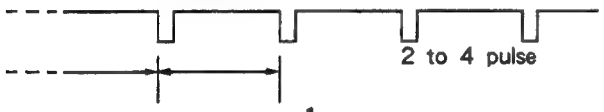
In the RESTART RESET (R.R) mode, information for one screen can be retrieved at any time. It is necessary to internally set the R.R mode in the camera to provide the R.R mode. See Section 2 - 5. "OPERATION MODE SETTING".
Supply the HD and R.R signals to pin 6 and pin 7 of the 12-pin connector to obtain output.

**Input conditions for the HD and R.R signals**

- Frequency(period)

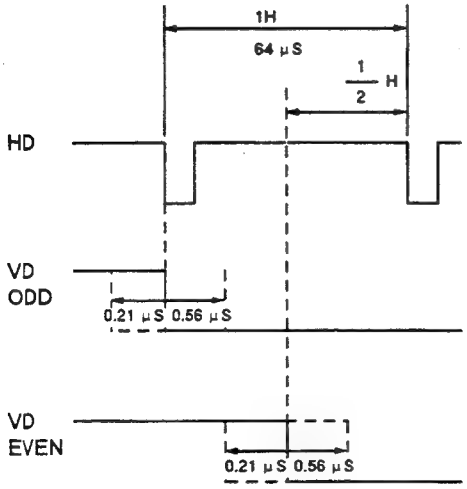
HD signal : 15.625 kHz ± 1% (64 μs ± 1%)
Continuous pulse


VD signal : 294 to 1023 1/2 H
2 to 4 pulses depending on the mode




Any time interval $294 \sim 1023\frac{1}{2}$ H

- Phase




- For the phase relation between external input HD and VD pulses, the allowance for the center phase in the specification is +8 clocks and - 3 clocks (maximum) as shown in the figure above.

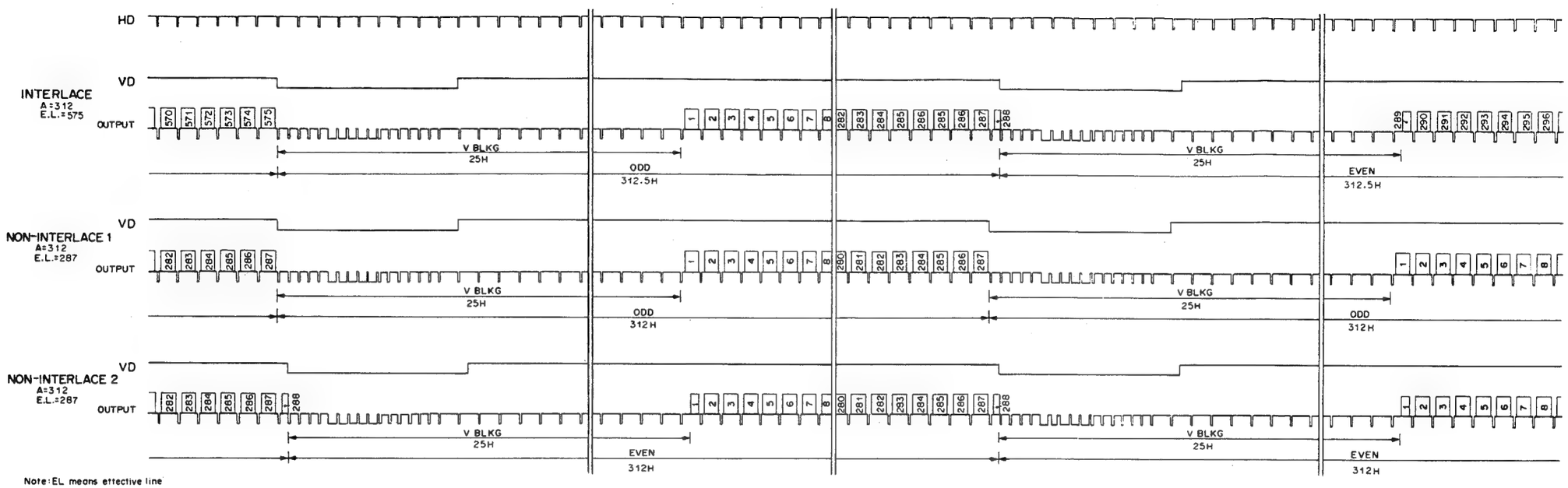
**Explanation of the timing chart**

Figure 3 is the timing charts for each operation mode. The details of these timing charts are given below:

- Frame integration interlace mode
  The R.R requires four pulses. Set the period of the R.R to (A + 1/2)H. A is an integer, 294 to 1023. It is 312 in the figure.
  Shooting information during STORAGE 1 and STORAGE 2 is output in the intervals of IMAGING C (ODD) and IMAGING D (EVEN). The CCD is reset in the intervals of IMAGING A and IMAGING B. Therefore, signals output during these intervals are meaningless.

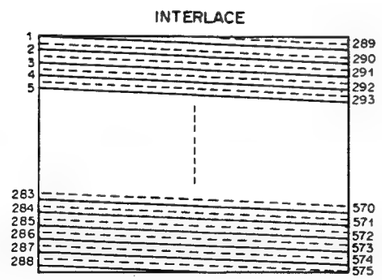
- Field integration interlace mode
  The R.R requires three pulses. Set the period of the R.R to (A + 1/2)H. A is an integer, 294 to 1023. It is 312 in the figure.
  Shooting information during STORAGE 1 and STORAGE 2 is output in the intervals of IMAGING B (ODD) and IMAGING C (EVEN). The CCD is reset in the interval of IMAGING A; therefore, signals output during this interval are irrelevant.

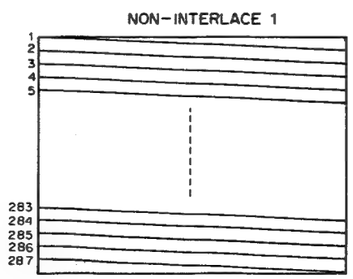
- Non-interlace mode
  The R.R requires two pulses regardless of the storage mode. Set the period of the R.R to A H. A is an integer, 294 to 1023. It is 312 in the figure.
  Shooting information in STORAGE 1 is output in the interval of IMAGING B. The CCD is reset in the interval of IMAGING A; therefore, signals output during this period are irrelevant.

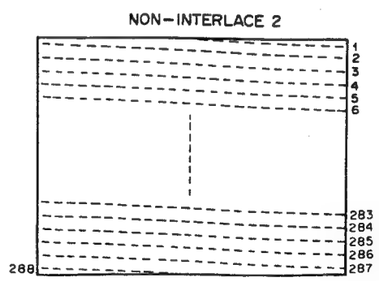



Note: EL means effective line

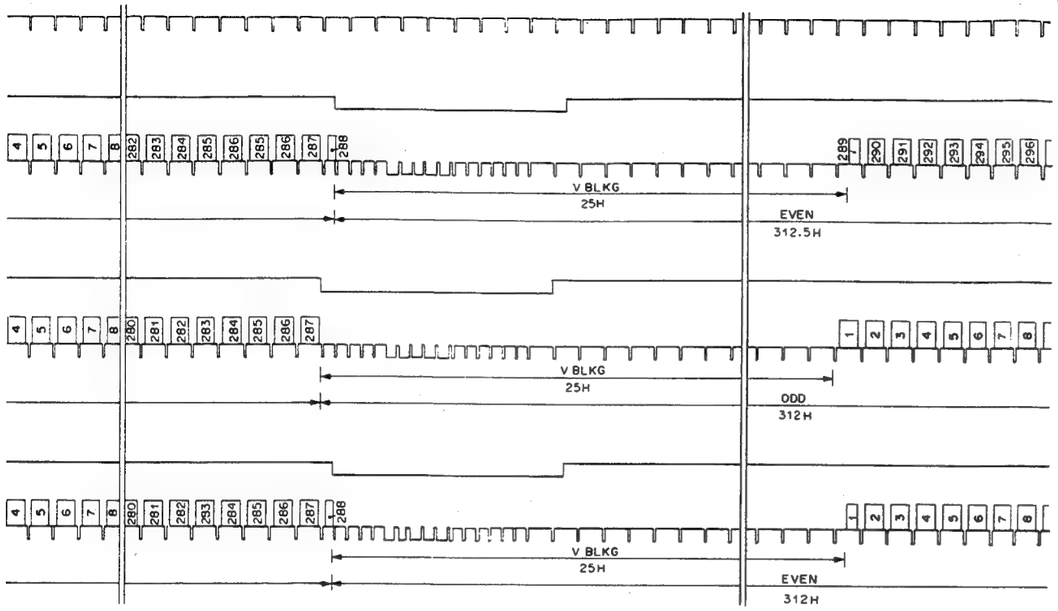
| | |
|---|---|
| Read out mode setti | |
| Scanning mode | |
| Scanning | NORMAL MODE |
| | INVERSE MODE |
| Storage time and VIDEO OUT correlat | |
| Vertical effective li (TV lines) | |
| RESTART RESET | |
| Features and application | |



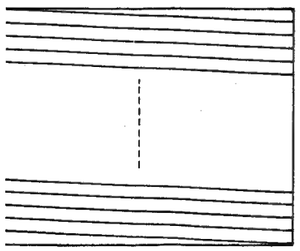




[Fig. 1]

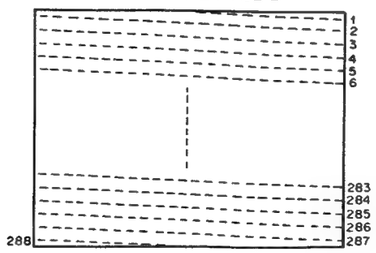



NON-INTERLACE 1

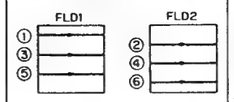
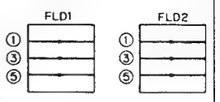
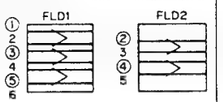
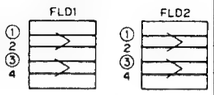
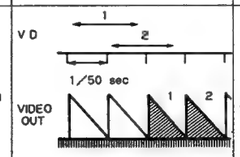
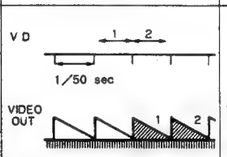
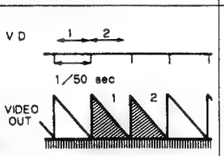
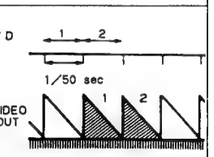
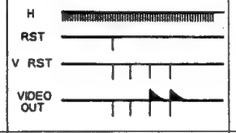
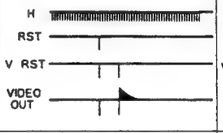
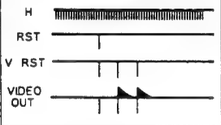
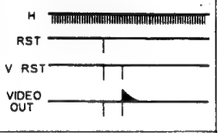


[Fig. 1]

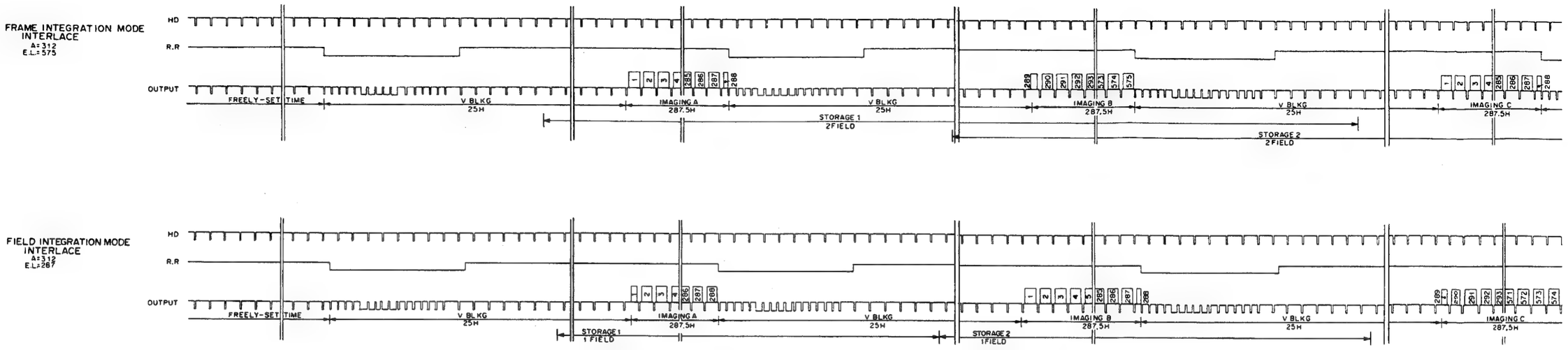
NON-INTERLACE 2



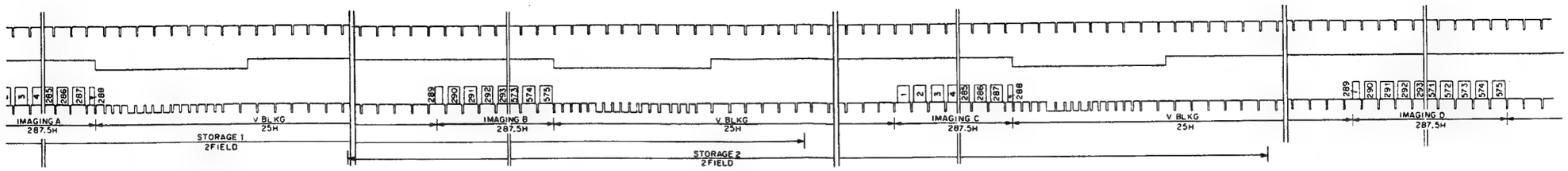


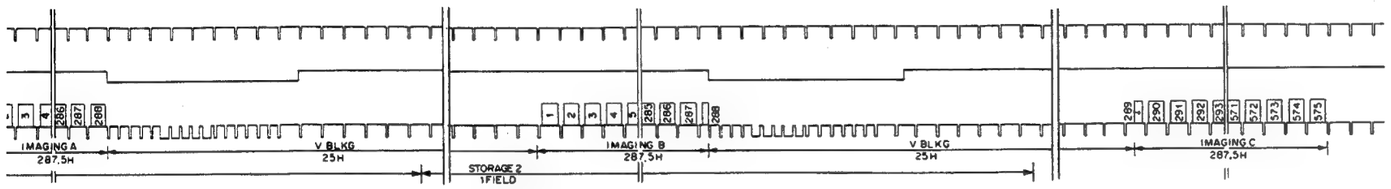

| Read out mode setting | | Frame integration mode (XC-73CE/75CE initial setting) | | Field integration mode | |
|---|---|---|---|---|---|
| Scanning mode | | Interlace | Non-interlace | Interlace | Non-interlace |
| Scanning | NORMAL MODE |  |  |  |  |
| | INVERSE MODE | FLD 1 and FLD 2 are inverted. | FLD 1 and FLD 2 become ②, ④, ⑥.... | FLD 1 and FLD 2 are inverted. | FLD 1 and FLD 2 become ②, ④, ⑥.... |
| Storage time and VIDEO OUT correlation | |  |  |  |  |
| Vertical effective lines (TV lines) | | 575 | 287 | 400 | 287 |
| RESTART RESET | |  |  |  |  |
| Features and application | | As the highest possible resolution is obtained, it is adapted to the measurements of the frame memory. | Same system as XC-39. Operates per 1 vertical line. Note: The operation is field integration mode. | Due to the storage of 1/50 seconds, a picture with even less disturbances than the frame integration mode is obtained. Adapted to pick up a moving object. | This system obtains all the vertical information without decreasing the sensitivity in non-interlace mode. |

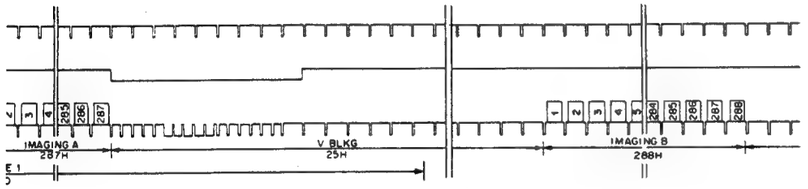
[Fig. 2] Relation between scanning mode and integration mode

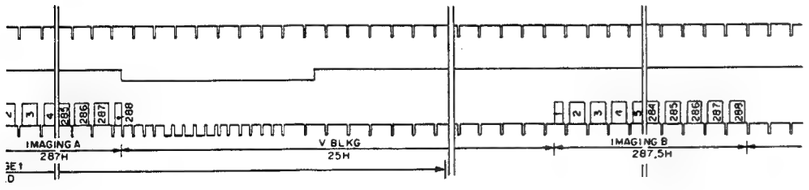

FRAME INTEGRATION MODE
INTERLACE
A=312
E.L=575
HD
R.R
OUTPUT
FREELY-SET TIME
V BLKG
25H
IMAGING A
287.5H
STORAGE 1
2FIELD
IMAGING B
IMAGING C
STORAGE 2
FIELD INTEGRATION MODE
INTERLACE
A=312
E.L=287
STORAGE 1
1 FIELD
STORAGE 2
NON-INTERLACE 1
A=312
E.L=287
OUT PUT
IMAGING A
287H
IMAGING B
288H
NON-INTERLACE2
A=312
E.L=287
IMAGING A
287H
IMAGING B
287.5H

[Fig. 3]


IMAGING A
287.5H
V BLKG
25H
STORAGE 1
2FIELD
IMAGING B
287.5H
V BLKG
25H
STORAGE 2
2FIELD
IMAGING C
287.5H
V BLKG
25H
IMAGING D
287.5H


IMAGING A
287.5H
V BLKG
25H
STORAGE 2
1FIELD
IMAGING B
287.5H
V BLKG
25H
IMAGING C
287.5H


IMAGING A
287H
V BLKG
25H
IMAGING B
288H


IMAGING A
287H
V BLKG
25H
IMAGING B
287.5H

[Fig. 3]

## 2-5. OPERATION MODE SETTING

The operation mode of the XC-73CE/75CE can be selected as required.
Each mode is set using a switch or soldering jumper.

| No. | Item | Location | Setting | Factory-setting mode |
|---|---|---|---|---|
| 1 | γ correction mode | PR-165 Board | Jumper JR1, JR2*1 | OFF |
| 2 | Electronic shutter mode | MB-403P Board | Jumper JR1 | OPEN(NORMAL) |
| 3 | Shutter control pulse setting | MB-403P Board | Jumper JR2 | OPEN |
| 4 | Normal electronic shutter speed setting | MB-403P Board | Switch S1 | "0"(OFF) |
| 5 | Charge accumulation mode | MB-403P Board | Jumper JR3 | OPEN(FRAME) |
| 6 | Sync signal input/output (HD/VD) | SG-199P Board | Switch S1 | EXT(INPUT) |
| 7 | EXT-HD termination (ON/OFF) | SG-199P Board | Switch S2 | ON |
| 8 | EXT-VD termination (ON/OFF) | SG-199P Board | Switch S3 | ON |
| 9 | H phase advance* | SG-199P Board | Jumper JR1 to 6 | Only JR1 and JR2 are short circuit. |
| 10 | RESTART-RESET mode* | SG-199P Board | Jumper JR7, 8 | SHORT(OFF) |
| 11 | FIELD INVERT mode* | SG-199P Board | Jumper JR9 | OPEN |
| 12 | GAIN mode | Rear panel | Switch | FIX |
| 13 | MANUAL GAIN | Rear panel | Volume control | 0 dB |
| 14 | Clock signal output | Rear panel | Jumper JR1 | OPEN |

* : The H phase advance, restart-reset, and field inversion can be set in only the external sync mode.
Each operation mode is described below.

*1 : In case the board suffix -11 of PR-165 board, the switch S1 mounted insted of JR1 and JR2.
Serial number ;
XC-73CE (EK) : 400001-405150
XC-75CE (EK) : 10001-53000

### 1. γ correction mode ( γ ON/ γ OFF)

A γ - corrected video signal is output when the γ correction mode is set to ON.

No γ correction is performed when this mode is set to OFF. Therefore, a video output signal proportional to the light intensity of an object can be obtained.

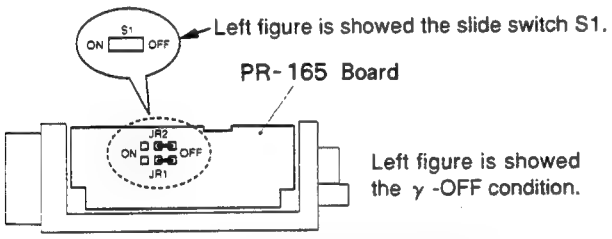
This correction mode is set using *internal jumpers JR1 and JR2 PR-165 board.

* In case the board suffix -11 of PR-165 board, the γ correction mode is set using slide switch S1.
  Serial number ;
  XC-73CE (EK) : 400001-405150
  XC-75CE (EK) : 10001-53000

It is set to γ OFF at the factory.

PR-165 board

| Mode | JR1, JR2 | S1 | input/output characteristic |
|---|---|---|---|
| γ ON (0.45) | ON : Short between the center land and the ON-side land. | ON | OUT / IN |
| γ OFF (1.0) | OFF : Short between the center land and the OFF-side land. | OFF | OUT / IN |

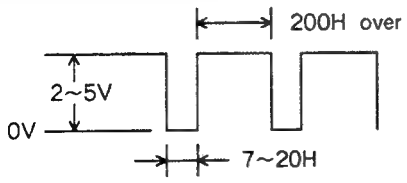



### 2. Electronic shutter mode (NORMAL/SPECIAL)

The electronic shutter mode sets the type of a CCD's electronic shutter.

- The NORMAL mode indicates an ordinary electronic shutter. The shutter speed is set using rotary switch S1 on the MB - 403P Board (described in No. 4).
- The SPECIAL mode indicates an electronic shutter that has an exposure start in random timing. An input pulse that determines the exposure start is selected using jumper land JR2 on the MB - 403P (described in No.3).

**Note)** Be sure to feed the two reset pulses to the 12-pin connector (pin7) after the power is just turned on.




| Mode | JR1 (MB - 403P) |
|---|---|
| NORMAL | OPEN |
| SPECIAL | SHORT |

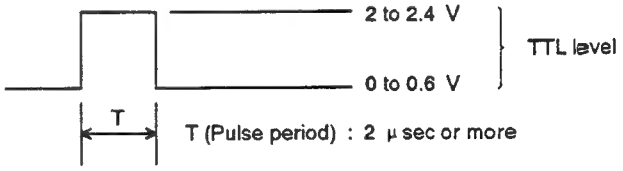
### 3. Shutter control pulse setting

This item selects an input pulse that determines the exposure start of an electronic shutter in the SPECIAL mode. VD and TR can be selected.

- If VD is selected, the falling edge of an internal VD pulse becomes the phase of a last shutter pulse just before an exposure start. Therefore, the exposure starts after about 2.0 μsec from this phase. The shutter speed is set according to the type and field of the CCD.
  (For the operation condition and timing chart, refer to the attached sheet.)
- If TR is selected, the rising edge of a pulse input from the 6 - pin connector (pin 2) on the rear panel becomes the phase of a last shutter pulse just before an exposure start. Therefore, the exposure starts after about 2.0 μ sec from this phase.
  The shutter speed is determined by the phase difference between the input pulse above and external sync VD pulse. It can be set freely.
  (For the operation condition and timing chart, refer to the attached sheet.)
- Controlling the shutter speed of an electronic shutter from the outside
  Set the electronic shutter mode to SPECIAL and set the input pulse to TR. In the state above, set switch S1 on the SG - 199P Board (described later) to INT and extract an internal HD/VD output pulse from the camera. A control pulse is generated using this pulse. The shutter speed can be set from the outside when the generated control pulse is input to the 6 - pin connector (pin 2) on the rear panel.

**[Specification of shutter control pulse]**

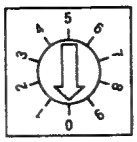
Input to a 6 - pin connector (pin 2) on the rear panel.




### 4. Normal electronic shutter speed setting

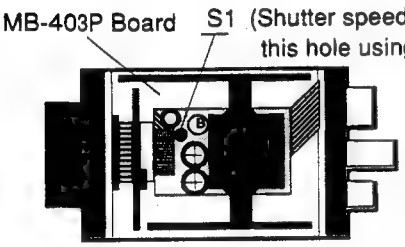
This item sets the electronic shutter speed in the NORMAL mode or sets the flicker - less mode. The electronic shutter speed and flicker - less mode are set using rotary code switch S1 on the MB - 403P Board.

| Position | Shutter speed |
|---|---|
| 0 | OFF |
| 1 | 1/125 |
| 2 | 1/250 |
| 3 | 1/500 |
| 4 | 1/1000 |
| 5 | 1/2000 |
| 6 | 1/4000 |
| 7 | 1/10000 |
| 8 | Flicker-less mode* |
| 9 | Flicker-less mode* |



Switch (S1) on the MB-403P board (Factory setting)

* : The flicker-less mode can be set when the rotary code switch is set to position 8 or 9. In positions 8 and 9, the shutter speed is 1/100 sec for EIA, and 1/120 sec for CCIR.




*Confirmation of Electronic Shutter OFF Position while Monitoring

**Condition:** Fix the lens iris.

Either of the two methods, described in a) and b) respectively, can be used to perform this confirmation.

a) Turn the rotary switch S1 on the MB-403P board clockwise and stop it where the image becomes brightest on the monitor. This detect position is the Shutter OFF position.

b) Turn the rotary switch S1 on the MB-403P board in the clockwise direction until the brightness of the image remains unchanged over two consecutive positions. Turn the switch one position farther. This is the shutter OFF position.

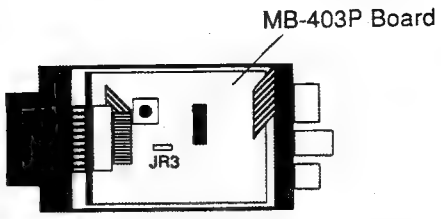
**5. Charge accumulation mode**

The accumulation mode sets the period in which signal charges are read from a CCD photosensor.

The accumulation mode is set using a jumper land JR3 (FLD) on the MB-403P Board. FLD is set to FIELD when it is short circuit. FLD is set to FRAME when it is opened.

- When the accumulation mode is set to FIELD, it enters the field accumulation mode in which signal charges are simultaneously read from the pixels in group 2.
- When the accumulation mode is set to FRAME, it enters the frame accumulation mode in which signal charges are alternately read from the pixels in group 2.
- In the frame accumulation mode, the sensitivity during noninterlaced scanning is one half of that during interlaced scanning. (Refer to Fig. 2 on page 2-11.)

The accumulation mode is set to FRAME at the factory.




**6. Sync signal input/output (HD/VD)**

This item sets whether a sync signal is output to the outside or input from the outside.

The external and internal sync modes are set using switch S1 on the SG-199P Board.

To set EXTERNAL mode, set switch S1 to the "E" side.

To set INTERNAL mode, set it to the "I" side

In case the board suffix -11 and -12 of SG-199P board, "EXT" and "INT" are printed on the board.

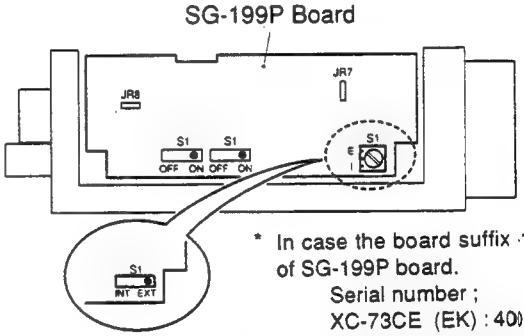
Serial number

XC-73CE (EK) : 400001-405150

XC-75CE (EK) : 10001-53700

- A video output signal synchronized with the sync signals (HD and VD signals) input from the outside is obtained when EXTERNAL (internal sync mode) is set.
- A sync signal that is generated internally can be output to the outside when INTERNAL (internal sync mode) is set.

Factory setting is EXTERNAL (external sync mode) .




* In case the board suffix -11 and -12 of SG-199P board.

Serial number ;

XC-73CE (EK) : 400001-405150

XC-75CE (EK) : 10001-53700

Changing the external sync input impedance

| * For high impedance input | | |
|---|---|---|
| SG-199P board | | |
| S2 | OFF | HD signal |
| S3 | OFF | VD signal |

Outputting the internal sync signals "HD" and "VD"

| SG-199P board | | |
|---|---|---|
| S1 | INT | |
| S2 | OFF | HD signal |
| S3 | OFF | VD signal |

### 7. EXT - HD termination (ON/OFF)

The HD input signal from the outside is terminated in 75 ohms. The 75ohm termination is set using switch S2 on the SG - 199P board. To terminate in 75 ohms, set switch S2 to ON. If not so, set switch S2 to OFF.

**Notes :** If switch S2 is set to OFF, a high impedance of more than 100K ohms is received.
To get the HD output signal, set switch S2 to OFF.

### 8. EXT - VD termination (ON/OFF)

The VD input signal from the outside is terminated in 75 ohms. The 75ohm termination is set using switch S3 on the SG - 199P Board. To terminate in 75 ohms, set switch S3 to ON. If not so, set switch S3 to OFF.

**Notes :** If switch S3 is set to OFF, a high impedance of more than 100K ohms is received.
To get the VD output signal, set switch S3 to OFF.

### 9. H phase advance

The phase of an internally generated HD signal can be advanced relative to the phase of an HD signal input from the outside during external HD/VD synchronization. The phase advance is set using jumper lands JR1 through JR6 on the SG - 199P Board.

| Jumper land | H phase advance |
|---|---|
| JR1 | 1 bit |
| 2 | 2 |
| 3 | 4 |
| 4 | 8 |
| 5 | 16 |
| 6 | 32 |

1 bit ≒ 70 ns

**Example :** A phase advance of 1 µsec is obtained by the expression below.
1000 ns ÷ 70=14.3

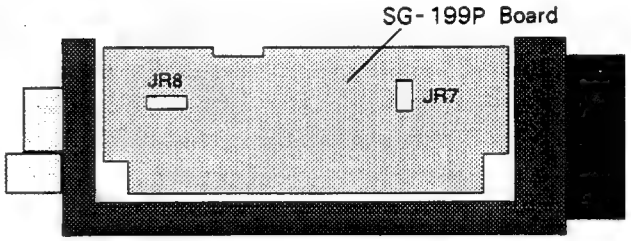
- In this case, if jumper lands JR2 through JR4 are short - circuited, the phase advance below can be set.
  2+4+8=14 bit × 70=980 ns=0.98 µs
- If jumper lands JR1 through JR4 are short - circuited, the phase advance below can be set.
  1+2+4+8=15 bit × 70=1050 ns=1.05 µs

Jumper lands JR1 and JR2 are set to the short - circuit state at the factory.

### 10. RESTART/RESET mode (R.R mode)

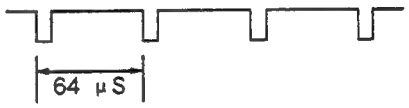
The RESTART/RESET mode fetches one - screen information in the external sync mode at any time.
The RESTART/RESET mode is set using jumper lands JR7 and JR8 on the SG - 199P Board.

| Jumper land | NORMAL | R.R |
|---|---|---|
| JR7 | SHORT | OPEN |
| JR8 | SHORT | OPEN |

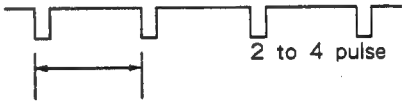



External sync input signal is required if the R.R mode is selected. The video signal is output by adding the HD signal to pin 6 of 12 - pin connector and the R.R signal to pin 7 respectively.

**Conditions : HD/R.R level 2 to 5 Vp - p**
Frequency(period)
HD signal : 15.625 kHz ± 1% (64 µs ± 1%)
Continuous pulse



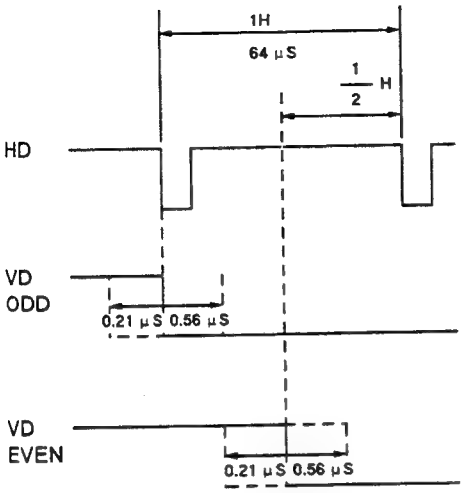

VD signal : 294 to 1023 1/2 H
2 to 4 pulses (depending on the mode)




Any time interval $294 \sim 1023\frac{1}{2}$ H

- The HD pulse is input continuously.
- The VD pulse can be input in any timing if the phase relation between the VD and HD pulses meets the specification (below).

• Phase




• For the phase relation between external input HD and VD pulses, the allowance for the center phase in the specification is +8 clocks and - 3 clocks (maximum) as shown in the figure above.
Jumper lands are set to NORMAL at the factory.

| FRAME accumulation | | FIELD accumulation | |
|---|---|---|---|
| interlaced | non-interlaced | interlaced | non-interlaced |
| R.R pulse | | | |
| 4 | 2 | 3 | 2 |

### 11. FIELD INVERT mode

The FIELD INVERT mode sets the field inversion of a video output signal when an external sync signal is input.
The FIELD INVERT mode is set using jumper land JR9 on the SG-199P board. It is set to INVERSE when JR9 is short-circuited, and set to NORMAL when JR9 is opened.

- If the FIELD INVERT mode is set to INVERSE, the field of the video output signal is inverted for the external sync signal. An even signal is output when the field of the external sync signal is odd. An odd signal is output when it is even.
- If the FIELD INVERT mode is set to NORMAL, the field of the video output signal is the same as during ordinary external synchronization. An odd signal is output when the field of the external sync signal is odd. An even signal is output when it is even.

The FIELD INVERT mode is set to NORMAL with JR9 opened at the factory.

### 12. GAIN mode (AUTO/FIX/MANUAL)

The GAIN mode sets the gain of a video output signal.
If the GAIN mode is set to AUTO, an automatic gain control (AGC) function is activated. The maximum gain of the automatic gain control is +18 dB.
In the MANUAL mode, the gain can be changed in the range of 0 to +18 dB using the volume control on the rear panel.

| Display | Mode |
|---|---|
| A | AUTO GAIN |
| F | FIX GAIN |
| M | MANUAL GAIN |

The GAIN mode is set to FIX GAIN at the factory.

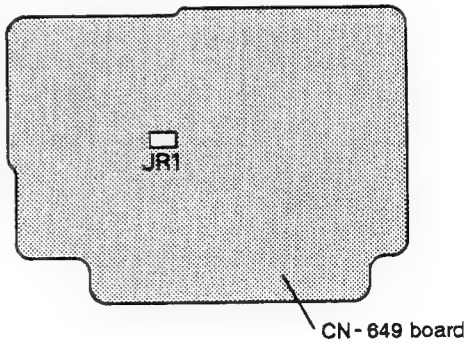
### 13. MANUAL GAIN control

The gain of a video output signal can be changed when the GAIN mode described above is set to MANUAL GAIN.
Minimum : 0 dB
Maximum : +18 dB
The gain of the video output signal is set to 0 dB at the factory.

### 14. CLOCK OUTPUT MODE

To obtain the clock signal output, short-circuit the jumper land JR1 on the CN-649 board.
The clock signal is output at pin 9 of 12-pin camera connector.

| Output Level | 5Vp-p |
|---|---|
| Output Impedance | 75 Ω |



## SPECIAL mode setting (1)

| | Fixed | Optional |
|---|---|---|
| Timing | ○ | – |
| Speed | ○ | – |

- To set up the SPECIAL mode setting (1) , confirm or set the jumper lands according to the following tables.
  (A figure showing the board locations of the jumpers necessary for the special mode setting is given on page 2-25 (E) .)

- MB-403P Board

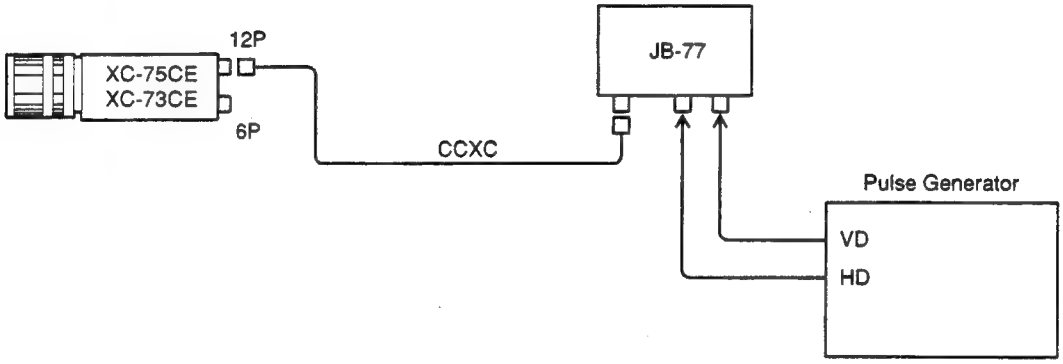
| | |
|---|---|
| JR1 | SHORT |
| JR2 | SHORT(VD) |
| JR3* | SHORT |

- SG-199P Board

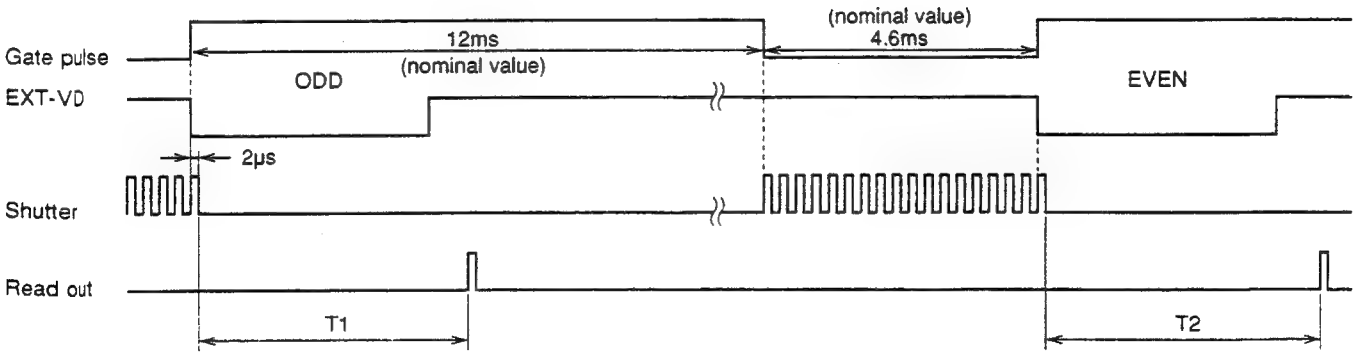
| | |
|---|---|
| S1 | EXT |
| JR7 | SHORT |
| JR8 | SHORT |

* When jumper land is shorted, FIELD mode is available. When jumper land is opened, FRAME mode is available, but the sensitivity becomes half level.

- Connection




- Pulse timing chart




| STANDARD | FIELD | EXPOSURE TIME | SHUTTER SPEED |
|---|---|---|---|
| EIA | T1 | 9H+42.2 μs | 1/1630 s |
| | T2 | 8.5H+42.2 μs | 1/1720 s |
| CCIR | T1 | 14.5H+43.3 μs | 1/1030 s |
| | T2 | 14H+43.3 μs | 1/1070 s |

**SPECIAL mode setting (2)**

| | Fixed | Optional |
|---|---|---|
| Timing | – | ○ |
| Speed | ○ | – |

- To set up the SPECIAL mode setting (2) , confirm or set the jumper lands according to the following tables.
  When this setting is executed, camera mode is changed to R.R mode from normal mode.
  (A figure showing the board locations of the jumpers necessary for the special mode setting is given on page 2-25 (E) .)

- MB-403P Board

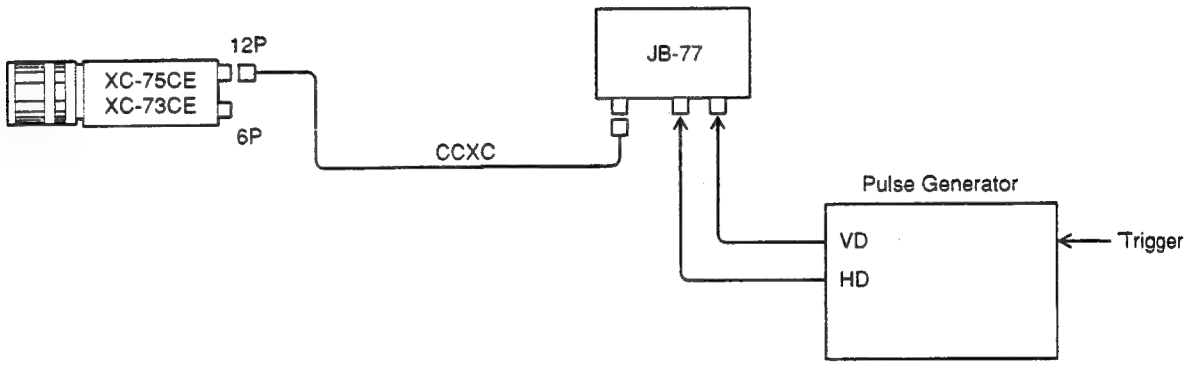
| | |
|---|---|
| JR1 | SHORT |
| JR2 | SHORT(VD) |
| JR3* | SHORT |

- SG-199P Board

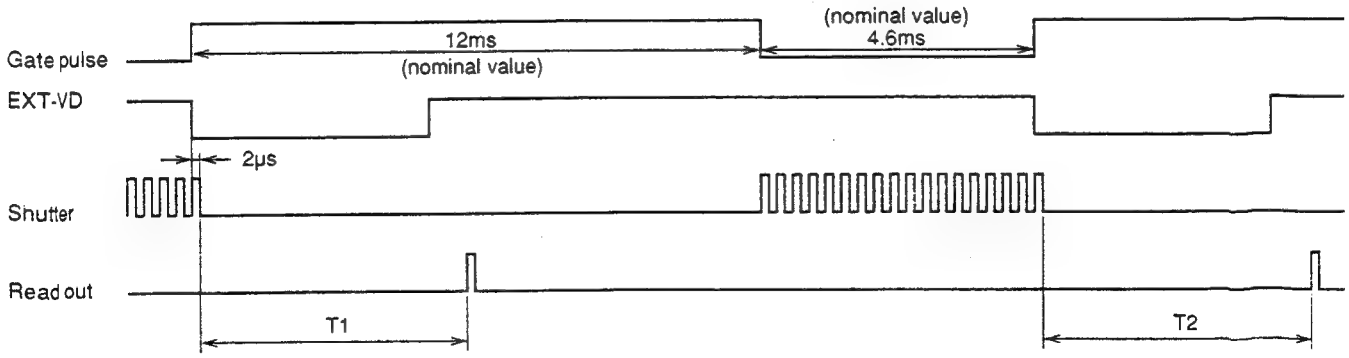
| | |
|---|---|
| S1 | EXT |
| JR7 | OPEN |
| JR8 | OPEN |

* When jumper land is shorted, FIELD mode is available. When jumper land is opened, FRAME mode is available, but the sensitivity becomes half level.

- Connection




- Pulse timing chart




- For more details of T1, refer to SPECIAL mode setting (1).
- A VD pulse must be latched by an HD pulse because of the R.R mode.

**SPECIAL mode setting (3)**

| | Fixed | Optional |
|---|---|---|
| Timing | – | ○ |
| Speed | – | ○ |

- To set up the SPECIAL mode setting (3) , confirm or set the jumper lands according to the following tables.
  When this setting is executed, camera mode is changed to R.R mode from normal mode.
  (A figure showing the board locations of the jumpers necessary for the special mode setting is given on page 2-25 (E) .)

- MB-403P Board

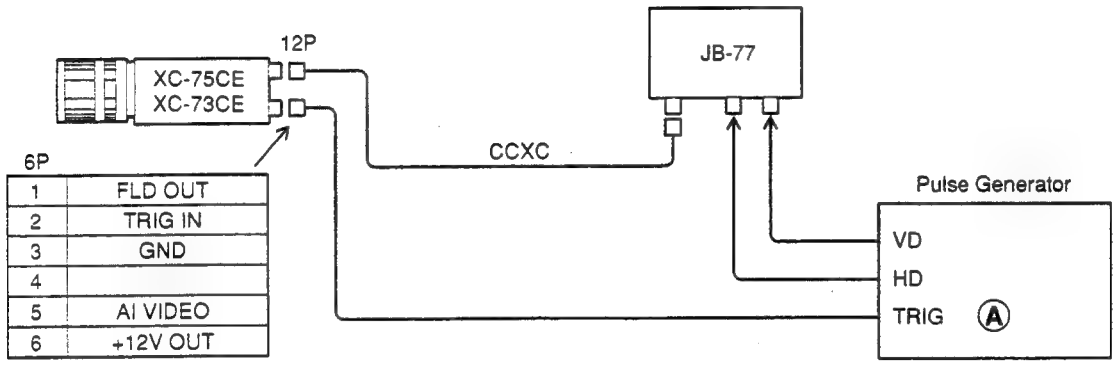
| | |
|---|---|
| JR1 | SHORT |
| JR2 | SHORT(TR) |
| JR3* | SHORT |

- SG-199P Board

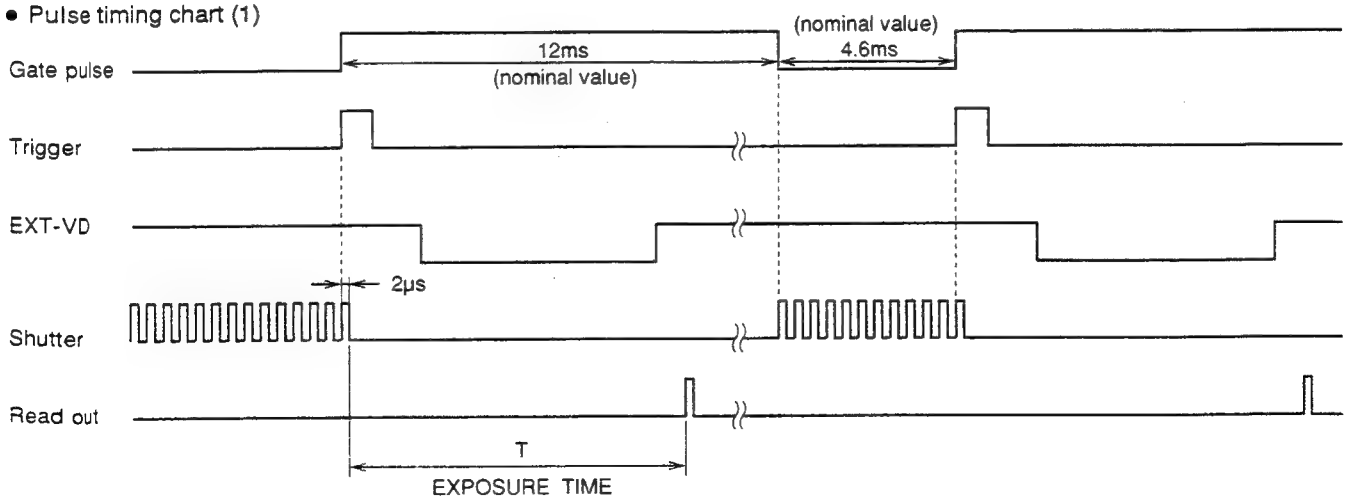
| | |
|---|---|
| S1 | EXT |
| JR7 | OPEN |
| JR8 | OPEN |

* When jumper land is shorted, FIELD mode is available. When jumper land is opened, FRAME mode is available, but the sensitivity becomes half level.

- Connection

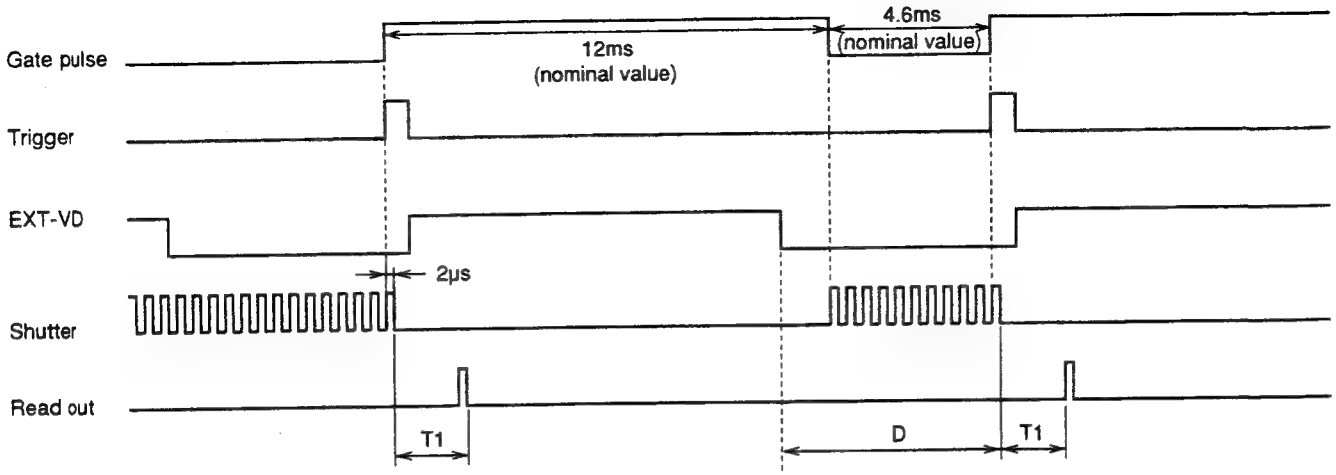



- Pulse timing chart (1)



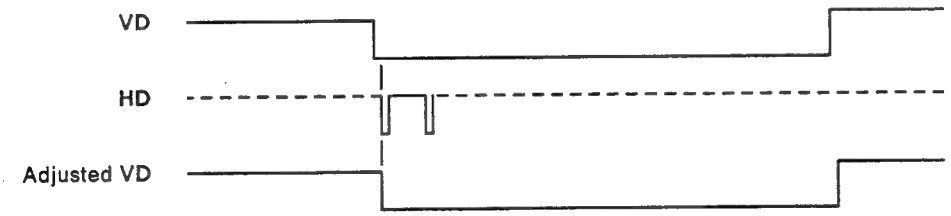

| STANDARD | FIELD | EXPOSURE TIME | SHUTTER SPEED |
|---|---|---|---|
| EIA | ODD | MAX 13 ms | 1/77 s |
| CCIR | EVEN | MAX 13 ms | 1/77 s |

● Pulse timing chart (2)




| STANDARD | FIELD | EXPOSURE TIME | SHUTTER SPEED |
|---|---|---|---|
| EIA | ODD | MIN 2 μs | 1/500000 s |
| CCIR | EVEN | MIN 2 μs | 1/500000 s |

**Notes :** 1. Adjust the VD pulse to the phase of the HD pulse because of the R.R mode.




2. For the shutter using an arbitray trigger, a VD pulse is usually generated after a trigger pulse. The maximum shutter speed below is thus obtained.
   EIA : 1/1548 s
   CCIR : 1/997 s
3. The extra-high shutter speed below id obtained when a trigger pulse is delayed relative to a VD pulse.

| STANDARD | FIELD | EXPOSURE TIME | SHUTTER SPEED |
|---|---|---|---|
| EIA | T1 | (9H+42.2 μ s) - D | MIN 1/500000 s |
| CCIR | T1 | (14.5H+43.3 μ s) - D | MIN 1/500000 s |

D : Delay of trigger pulse relative to VD pulse.

**SPECIAL mode setting (4)**

(Application of a shutter speed to the external control)

To set up the SPECIAL mode setting (4) , confirm or set the jumper lands according to the following tables.
(A figure showing the board locations of the jumpers necessary for the special mode setting is given on page 2-25 (E) .)

● MB-403P Board

| | |
|---|---|
| JR1 | SHORT |
| JR2 | SHORT(TR) |
| JR3* | SHORT |

● SG-199P Board

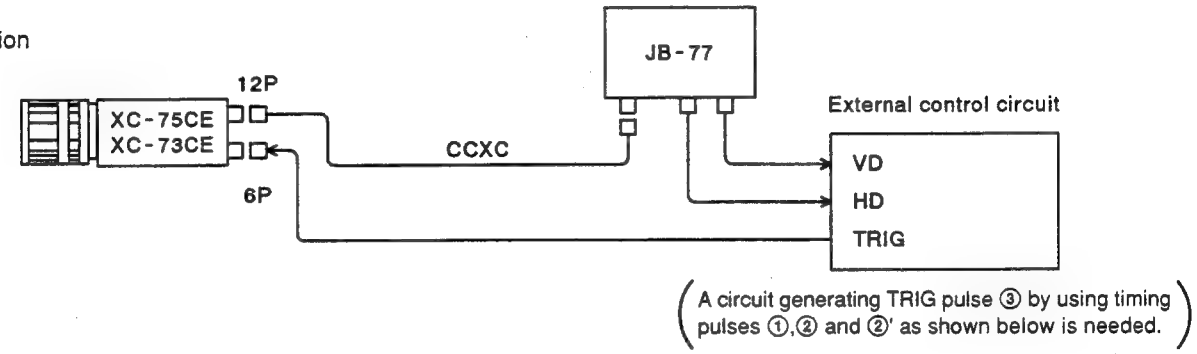
| | |
|---|---|
| S1 | INT |
| JR7 | SHORT |
| JR8 | SHORT |

● SG-199P Board

| | |
|---|---|
| S2 | OFF |
| S3 | OFF |

* When jumper land is shorted, FIELD mode is available. When jumper land is opened, FRAME mode is available, but the sensitivity becomes half level.

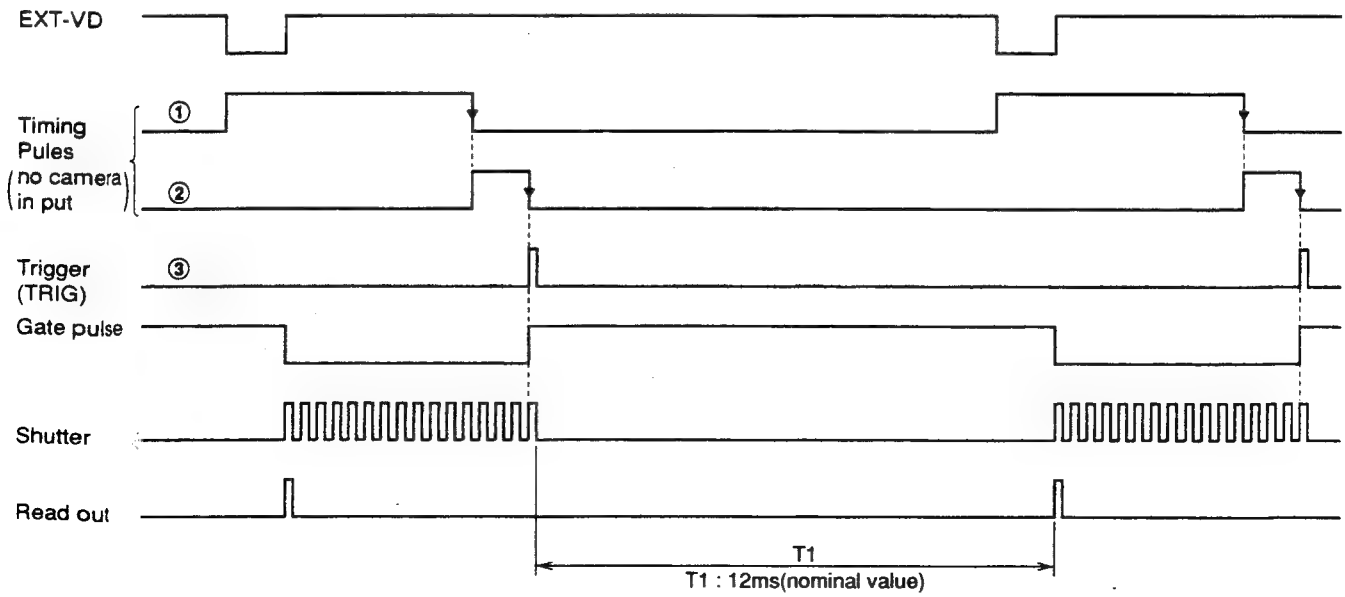
● Connection



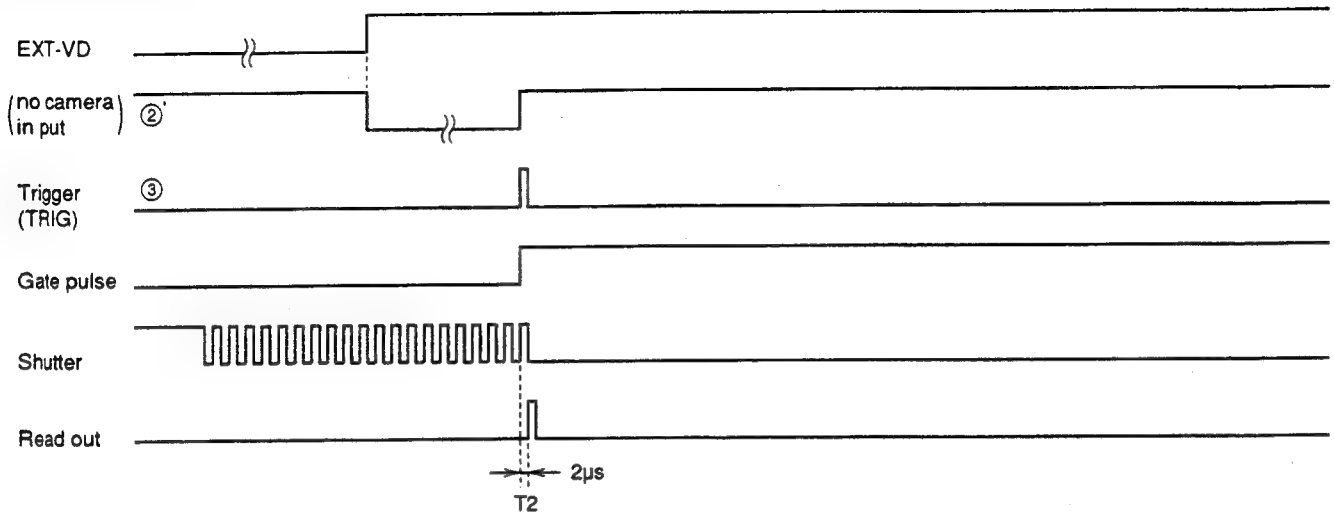

(A circuit generating TRIG pulse ③ by using timing pulses ①,② and ②' as shown below is needed.)

● Pulse timing chart (Exposure time : T1 through T2 can be changed continuously.)

Long time exposure

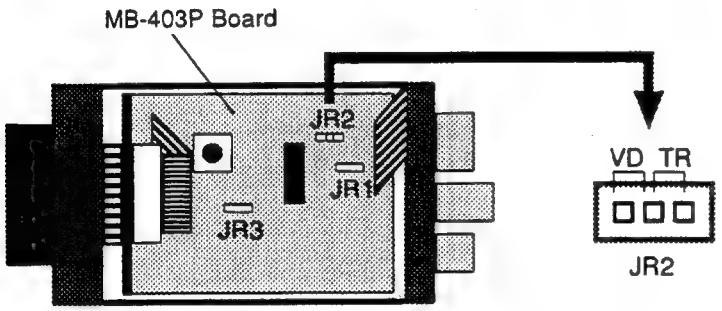


Short time exposure

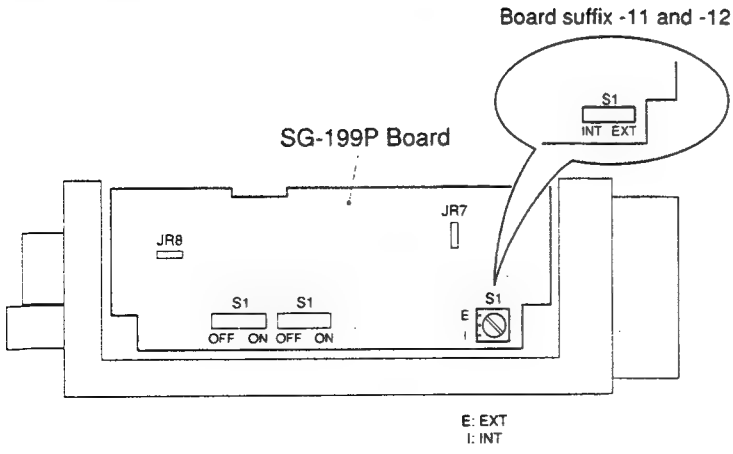



**BOARD LOCATION for SPECIAL mode setting**

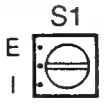
- MB-403P board




- SG-199P board




Note ;
Do not set S1 switch to mechanical center because that abnormal operation will be caused if S1 is set to mechanical center.




This is bad setting.

## 2-6. THEORY OF OPERATION

### 2-6-1. Operation Theory of CCD

A CCD (Charge-Coupled Device) image sensor consists of a regularly laid-out MOS (Metal-Oxide-Semiconductor) capacitor. The MOS capacitor has three basic functions below that treat a charge.

1. Photoelectric Conversion (Photosensor)
   When incident light falls on the MOS capacitor, the charge is generated in proportion to the illumination received.
2. Charge Storage
   When a voltage is applied to the electrode of a MOS capacitor, a "potential well" is generated in the silicon layer. The charge is stored in this well.
3. Charge Transfer
   When a higher voltage is applied to the electrode, a deeper well is generated. When a lower voltage is applied, a shallower well is generated.
   The charge is transferred using this characteristic. When a higher voltage is applied to the electrode, a deeper "potential well" is generated. The charges accumulated in an adjacent well flows into the "potential well". When this operation is sequentially repeated in the regularly laid-out electrode, the charge is transferred from one MOS capacitor to another MOS capacitor. This is the theory of the CCD charge transfer.

### 2-6-2. Structure of CCD Charge Transfer

In the interline transfer system that the XC-75CE and the XC-73CE use, the charge corresponding to the brightness of an image formed on a CCD image sensor is sequentially transferred as shown in Fig. 3 on page 2-27. The charge corresponding to the brightness of an object detected using a photosensor is first transferred to an adjacent vertical transfer register. The charge transferred to the vertical transfer register is sequentially transferred to a horizontal transfer register in the vertical direction. The charge transferred to the horizontal transfer register is sequentially transferred in the horizontal direction and output from the output stage.

**1. Vertical Transfer**

The vertical transfer register transfers a charge by four-phase driving. Fig.1 shows the state of a "potential well" at each time.

In the state of time t0, the electrode voltage is (V1 = V2) > (V3 = V4). Therefore, the well is deepened in the potentials of V1 and V2 with high voltage. The charge is stored in the deep well.

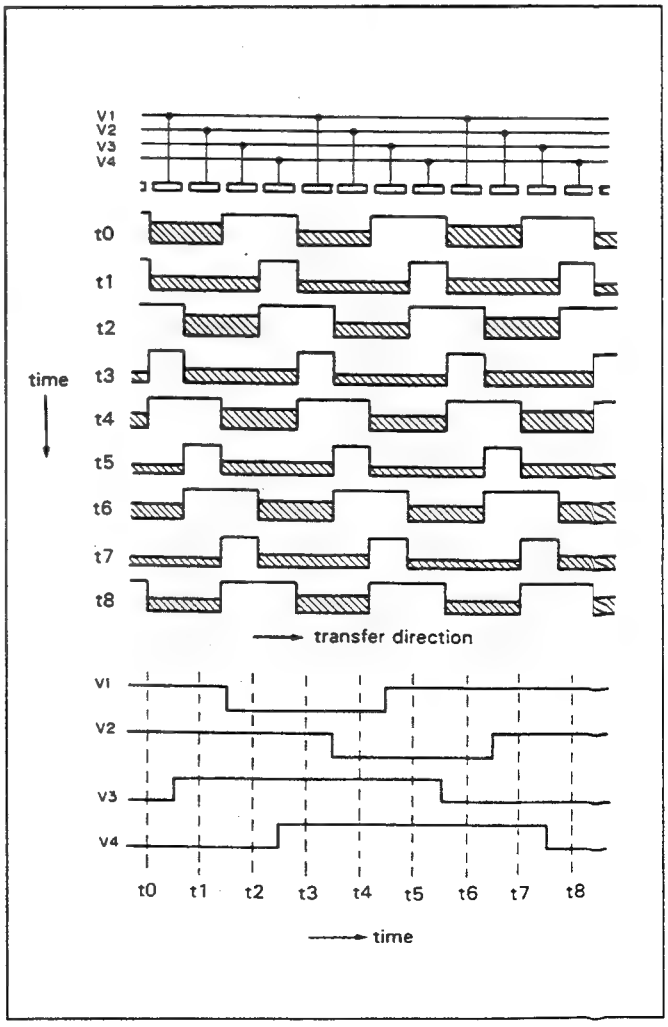
In time t1, the electrode voltage is (V1 = V2 = V3) > (V4). The charge is stored in the well of V1, V2, and V3.

In time t2, the electrode voltage is (V2 = V3) > (V4 = V1). The charge is stored in the well of V2 and V3.

The state of the electrode voltages in time t3 and later is described below.

| | |
|---|---|
| Time t3 | (V2 = V3 = V4) > (V1) |
| Time t4 | (V3 = V4) > (V1 = V2) |
| Time t5 | (V4) > (V1 = V2 = V3) |
| Time t6 | (V4 = V1) > (V2 = V3) |
| Time t7 | (V4 = V1 = V2) > (V3) |
| Time t8 | (V1 = V2) > (V3 = V4) |
| | (Same as the state of time t0.) |

This operation is sequentially repeated for the vertical transfer.




[Fig. 1] Vertical Transfer

## 2. Horizontal Transfer

The horizontal transfer register transfers a charge by two-phase driving. Fig. 2 shows the state of a "potential well" at each time.

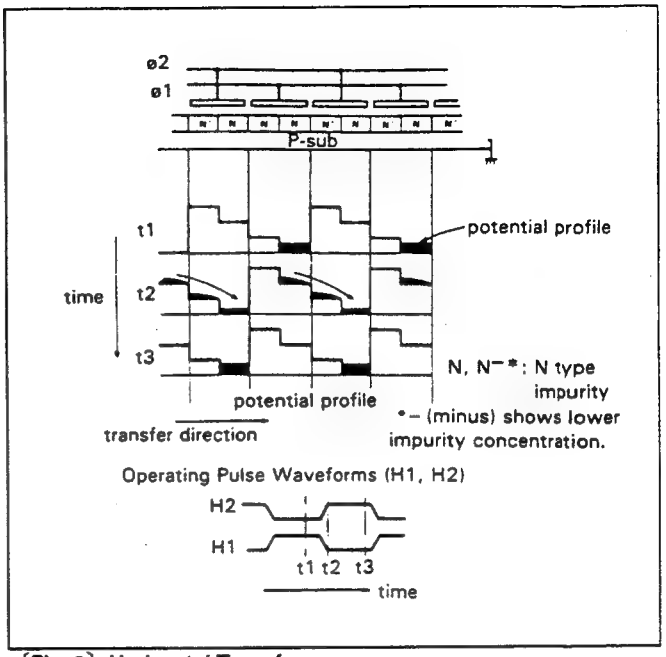
In the state of time t1, the electrode voltage is H1 > H2. Therefore, the well is deepened in the electrode of H1 with high voltage. The charge is stored in the deep well.

In the state of time t2, the voltage of H1 and H2 is inverted. The well of H2 becomes deep, and the well of H1 becomes shallow. The well of H2 becomes deeper than that of H1, so the signal charge flows into H2 with deeper well.

In the state of time t3, the electrode voltage does not change. The signal charge thus flows into the well of H2.

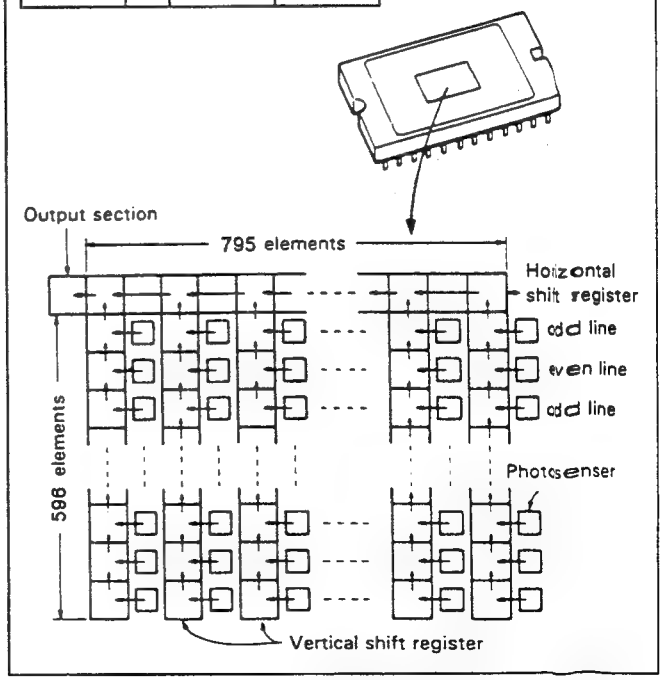
One charge transfer is then completed.

This operation is sequentially repeated for horizontal transfer.




(Fig. 2) Horizontal Transfer

| Standard | | Overall Picture Element | Effective Picture Element |
|---|---|---|---|
| EIA | H | 811 | 768 |
| | V | 508 | 494 |
| CCIR | H | 795 | 752 |
| | V | 596 | 582 |




(Fig. 3) The interline-transfer organization of the CCD image sensors

### 2-6-3. PA-147 Board (XC-75CE)
### PA-152 Board (XC-73CE)

The light passed through a camera lens strikes against the chip surface of IC1 (CCD image sensor) on the PA board.
An approximately 400,000 photosensors are arrayed on the CCD surface, and the incident light is converted into the charge corresponding to the brightness of light in a photosensor block.
The converted charge is stored in the photosensor for storage time to be set, then read to the transfer register.
The charge sequentially transferred to the transfer register is lastly output to the output stage of IC1 to produce a CCD output signal.
The output signal of IC1 is input through buffer amplifier Q3 to IC2 (CDS IC), where the noise component of the CCD output signal is reduced by correlative double sampling.
The resultant signal is output in the level that is about two times as high as an input signal.
The SHP and SHD pulses input to IC2 are a sampling pulse for correlative double sampling. The signal output from IC2 is output through buffer amplifier Q1 from the PA board and sent to the MB-403P Board.

### 2-6-4. MB-403P Board

The MB-403P Board mounts a timing pulse generator for CCD control and the circuit blocks below.

a. Timing pulse generator
b. Clock drive circuit for CCD vertical transfer
c. Electronic shutter control circuit
d. CCD-VSUB voltage control circuit
e. PB-BIAS voltage control circuit
f. System clock generator
g. Clock output driver
h. Video signal output driver

a. Timing pulse generator

Timing pulse generator IC3 generates timing pulses required for CCD driving by inputting a 28 MHz clock from the system clock generator and inputting HD and VD signals from the SG-199P Board.

| | |
|---|---|
| XPG | : Clock for CCD precharge gate |
| XH1, XH2, XLH1 | : Two - phase clock for CCD horizontal transfer |
| XV1 to XV4 | : Two - phase clock for CCD vertical transfer |
| XSUB | : Electronic shutter pulse |
| XSG1, XSG2 | : Charge read pulse from photosensor |

In addition, timing pulse generator IC3 generates the signal processing pulses below.

| | |
|---|---|
| SH1 | : Sampling pulse for correlative double sampling |
| SH2 | : Sampling pulse for correlative double sampling |
| CLP3 | : Clamp pulse for DC reproduction |

The timing pulse generator also outputs shutter pulse X-SUB whose generation period changes according to the output of rotary code switch S1, and sends it to the electronic shutter control circuit described later.

b. Clock drive circuit for CCD vertical transfer
Clock driver circuit for CCD vertical transfer IC1 inputs the CCD vertical transfer clock pulses (V1 through V4) from IC3 and the signal charge read pulses (SG1 and SG2) from a photosensor and outputs pulses V1 through V4 with SG1 and SG2 added to V1 and V3.
In this case, IC1 functions as the driver of pulses V1 through V4 so that it can directly drive the CCD.
The V2 output pulse is sent to a charge pump consisting of D1, D2, C1, and C2 to produce a V-SUB DC voltage (approximately +25 V).

c. Electronic shutter control circuit
The electronic shutter control circuit consisting of IC4, IC5, and IC6 switches the electronic shutter mode (NORMAL/SPECIAL) and controls the SPECIAL shutter.
Jumper land JR1 is set to OPEN at the factory. In this state, IC6 for a SPECIAL shutter is in the reset state.
For the output signal of a shutter pulse selection circuit consisting of IC5, a NORMAL shutter pulse, that is, the X-SUB output pulse of IC3 is selected.
The output logic of IC4 is inverted when jumper land JR1 is set to SHORT. The reset of IC6 is then canceled. IC6 can operate for the trigger pulse or VD pulse from the 6-pin connector on the rear panel in this case (the VD or trigger pulse is selected using jumper land JR2). Simultaneously, the output pulse of IC6 is selected as the output signal of a shutter pulse selection circuit consisting of IC5. This enables the operation of the SPECIAL shutter.
The trigger pulse input from the 6-pin connector on the rear panel is input through waveform shaping circuit Q8 to IC6. IC6 outputs a LAST shutter pulse and shutter OFF control pulse with the trailing edge of a pulse generated at the collector of Q8 as reference.
The LAST shutter pulse output from pin 10 of IC6 is synthesized with the XV2 pulse from IC3 using IC5.
The output period of the LAST shutter pulse is limited using a shutter OFF control pulse output from pin 6.
The resultant LAST shutter pulse is sent to IC1 as a SPECIAL shutter pulse.

d. CCD-VSUB voltage control circuit
The CCD-SUB voltage control circuit consisting of Q12, Q13, D6, D7, C1, C41, and R45 through R51 provides a proper DC voltage varying with each CCD for the overflow drain (OFD) that prevents a CCD photosensor from overflow. Adjust this circuit using RV1 while reading the value at TP1.
The reference voltage (approximately +5 V) produced from +15 V is sent to pin 3 of Q12. Pin 5 of Q12 operates so that it is parallel to this voltage. The diode at pin 1 of D60 is a clamping diode that clamps a shutter pulse into the DC voltage at TP1. The clamping diode compensates for the temperature of the diode at pin 1 using a diode at pin 2 of D6.

e. PG-BIAS voltage control circuit
The PG-BIAS voltage control circuit consisting of R54, R55, C44, and RV2 adjusts the DC bias of a PG pulse sent to the CCD. Adjust this circuit using RV2 while reading the value at TP2.

f. System clock generator
The system clock generator consists of a crystal oscillator and L-C oscillator.
Whether to select the output signal (28 MHz) of the crystal oscillator or L-C oscillator is performed automatically.
When an external sync signal (HD/VD or VS) is input from the outside of a camera, a high-level signal (+5 V) is output to pin 12 of IC1 (CXD-1084) on the SG-199P Board. This control signal is sent to pin 9 of connector CN7 on the MB-403P Board to control a switch circuit consisting of logic circuit IC2. The output signal of the L-C oscillator is then selected as a clock output and sent to the input pin of IC3.
The L-C oscillator constitutes some circuits on the SG-199P Board and a phase-locked loop (PLL) circuit. The 28 MHz clock output from the L-C oscillator is frequency-divided using IC3 to produce a 14 MHz clock. The 14 MHz clock is sent through pin 7 of connector CN7 to the SG-199P Board and input to IC1 on the SG-199P Board. IC1 produces a camera's sync signal from the input clock. During external synchronization, an H SEP pulse obtained when the component of a horizontal sync signal is separated from the external sync signal is output. An H reference signal that is produced from this pulse and clock is input to phase comparator IC2 on the SG-199P Board. The component of the phase difference is output from IC2.

The output phase - difference component is sent to pin 10 of connector CN7 on the MB - 403P Board, passed through a low - pass filter consisting of R39, C36, and C39 on the MB - 403P Board, and sent to the cathode of D5. The capacity of D5 varies depending on the voltage supplied by a variable capacitor. Therefore, the oscillation frequency of the L - C oscillator consisting of IC2, R34, L6, C29, C30, C31, C43, CT1, and D5 changes. The loop is designed to control the oscillation of a clock that determines the phase of an H reference signal so that the phase difference between the H reference signal produced from a clock and the H SEP signal separated from an external sync signal is zero ("0").

CT1 is used to suppress the part variation. CT1 is set to operate in the center value (about +2.5 V cathode voltage of D5) of the PLL's variable range when the external sync signal in the center of the specification is input.

A low - level signal (0 V) is output to pin 12 of IC1 on the SG - 199P Board when no external sync signal is input from the outside of a camera. For the output signal of a system clock oscillator, the output signal of a crystal oscillator is selected using a switch consisting of logic circuit IC2.

g. Clock output driver

The clock output driver consisting of Q9, Q10, Q11, R40, R41, C38, and C39 is a class B bias push - pull type cable driver. It can drive a coaxial cable with 75 ohm characteristic impedance.

The 14 MHz clock output from pin 57 of IC3 is sent through this clock output driver to pin 16 of connector CN5.

h. Video signal output driver

The video signal processed on the PR - 165 board is input from pin 6 of connector CN1 and sent to a buffer amplifier consisting of Q14, R56, and R57. The signal passed through the buffer amplifier is sent to a 14 MHz trap filter consisting of FL2, R59, and R60 to eliminate the noise of a 14 MHz component, then input to the output driver circuit.

The output driver circuit consists of Q1 through Q5, Q7, R4 through R10, R15, R16, C6, C9, and C11. It has a voltage gain that is about 1.7 times as high as usually.

A push - pull type cable driver is located as the last stage. The cable driver can drive a coaxial cable with 75 ohm characteristic impedance. The video output signal is sent through this video signal output driver to pin 9 of connector CN5.

## 2-6-5. PR-165 Board

The PR-165 board processes the video signal obtained from CCD.

a. Fixed gain amplifier
b. Black tracking pulse generator
c. Process IC
d. Sync mix circuit

a. Fixed gain amplifier

The fixed gain amplifier consisting of Q1, Q3, Q5, R10, R14 through R18, R21, R23, C8, and C10 has a voltage gain of about two times as high as usually. A CDS-processed signal from pin 6 of connector CN1 is input to the fixed gain amplifier.

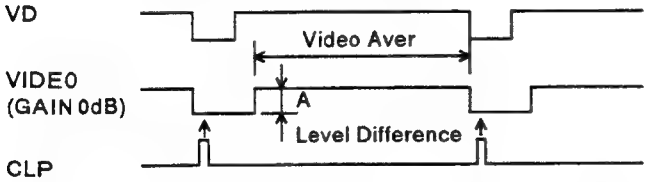
This amplifier is used to obtain a signal with high S/N ratio as the video output signal of a camera. When the GAIN mode switch on the rear panel is set to FIX, the video output signal on the RP-165 board is processed without passing through an amplifier incorporated into IC2, then output.

The gain of the amplifier incorporated into IC2 varies depending on the voltage control. The amplifier is also constituted by many transistors. Therefore, when a signal is passed through this portion, the S/N ratio of the amplifier slightly deteriorates as compared with the fixed gain amplifier above. The fixed gain amplifier is thus used to obtain a video signal with higher S/N ratio.

b. Black tracking pulse generator

The black tracking pulse generator is used to suppress the fluctuation in the black level of a video signal.

The black level of the video signal is DC-reproduced for processing using a clamp pulse. The resultant video signal is input to the processing circuit. When there is slightly a level difference between the clamp phase level and video black level, the level difference fluctuates if the gain of a video amplifier changes. Lastly, the black level fluctuates.




As shown in the figure above, if the difference between the clamp phase level and video black level is "A" when the gain is 0 dB, the level difference during 6 dB gain is 2 × A. The black level significantly floats because the clamp phase level is fixed. Therefore, analog switch IC1 is controlled using an HD signal to produce a correction pulse.

The produced correction pulse is sent to IC2 and the fixed gain amplifier and added to the video signal so that the fluctuation in the video black level using a gain disappears.

The correction pulse is produced using a circuit consisting of IC2, R4 through R9, C3, C6, C7, RV2, and RV3. The correction level for an IC2 pulse is set using RV2. The correction level for a fixed gain pulse is set using RV3.

c. Process IC

The major function of the Process IC is γ, white clip, and setup signal processing. The Process IC also outputs the video signal processed for an automatic gain control circuit and auto iris lens.

The video signal input from pin 6 of connector CN1 is input through buffer amplifier Q2 to IC2. The input signal of IC2 is first passed through an amplifier and output from IC2 once.

The amplifier in the first stage is a voltage control type of gain control amplifier. This amplifier is valid for a camera output signal when the GAIN mode switch on the rear panel is set to AUTO or MANUAL.

The CONT1 signal at pin 3 of connector CN2 is set high (+5 V) when the GAIN mode switch on the rear panel is set to AUTO or MANUAL. The output signal of analog switch IC3 then selects the output signal of gain amplifier IC2. The CONT2 signal at pin 2 of connector CN2 selects the control voltage of this gain amplifier. The output voltage of an AGC loop consisting of IC2 and external circuits (R27, R29, R33, R34, R37, R42, R43, C18, C19, C23, C25, Q7, and RV9) is selected when the GAIN mode switch is set to AUTO. The output level of a video signal is automatically kept constant for the change of incident light. The level of the video output signal is adjusted using RV9. The maximum gain is limited using RV10.

The CONT2 signal at pin 2 is set low when the GAIN mode switch is set to MANUAL. The control voltage input from pin 1 of connector CN2 is then selected as a gain amplifier control voltage. This voltage can be controlled by the volume control on the rear panel. The gain of the gain amplifier can be manually controlled by this volume control.

The video signal selected whether to be output from a fixed gain amplifier or gain amplifier IC2 is input through buffer amplifier Q10 to IC2 again.

The video signal input to IC2 is output via a γ correction circuit (GAM OUT) or output directly (LIN OUT). The GAM OUT signal is selected using switch S1 when γ is on. The LIN OUT signal is selected using switch S1 when γ is off. These signals are input through buffer amplifier Q6 to IC2 again. The video signal input to IC2 again is set up and white-clipped. The resultant video signal is output from IC2 lastly. The setup is performed using RV1 (γ :OFF) or RV4 (γ :ON), and the white clip is performed using RV5.

d. Sync mix circuit

The sync signal input from pin 5 of connector CN2 is level-adjusted using RV8. The adjusted sync signal is passed through buffer amplifier Q11 and mixed with a video signal. The video signal processed by IC2 is adjusted to the proper level using RV6. The adjusted video signal is sent to pin 6 of connector CN2 and output from the PR-165 board.

- In addition, a video signal for an auto iris lens is output from pin 27 of IC2. This video signal is sent through buffer amplifier Q9 to pin 4 of connector CN2 and output from the PR-165 board.

## 2-6-6. SG-199P Board

The SG-199P Board is connected to an MB board via board-to-board connector. It receives the clock from the MB board, produces various sync signals from the clock, and sends it to the MB board again.

The circuits on the SG-199P Board can be functionally classified into the blocks below.

a. Internal/external sync selection block
b. Sync signal generation block
c. Function set block
d. Phase comparison block

The operation for every block is described below.

a. Internal (*I)/external (*E) sync selection block

Switch S1 is used to select an internal or external sync signal output. By the setting of switch S1, +5 V is sent from the output pin of S1 as a control voltage during internal sync setting. -9 V is sent as a control voltage during external sync setting.

*1 This control voltage is input to a vertical sync signal selection circuit consisting of analog switches IC8 and IC9.

Besides, HD input/output signal is changed directly by switching S1.

* In case the board suffix -11 and -12 of SG-199P board, "EXT" and "INT" are printed on the board.

*1 [In case the board suffix -11 and -12 of SG-199P board] This control voltage is input to a horizontal sync signal selection circuit consisting of analog switches IC6 and IC7 and a vertical sync signal selection circuit consisting of analog switches IC8 and IC9.

- Internal sync signal output

*2 When switch S1 is set to "*I", +5 V is sent from the output pin of S1. Therefore, IC9 is turned on, and IC8 is turned off. The internal sync signal output mode is then selected.

The HD and VD signals output from sync signal generator IC1 are driven and HD signal is input to switch S1, also VD Signal inputs to analog switches IC9.

*2 [In case the board suffix -11 and -12 of SG-199P board] When switch S1 is set to INT, +5 V is sent from the output pin of S1. Therefore, IC7 and IC9 are turned on, and IC6 and IC8 are turned off. The internal sync signal output is then selected.

The HD and VD signals output from sync signal generator IC1 are driven and inputs to analog switches IC7 and IC9.

The drive circuit of the VD signal uses IC4.

For the HD signal, a circuit consisting of Q5, C24, R25, and R26 is used as the drive circuit so as to reduce the signal deterioration caused by the input resistance and capacity of analog switches during cable extension.

The HD and VD signals passed through analog switches are output from pins 5 and 6 of connector CN1, respectively.

Set S2 and S3 that external sync signal termination, to OFF postion for obtaining internal sync signal output.

The HD and VD signals are then passed through the MB and CN boards from the SG board and output from the connector on the rear panel to the outside of a camera.

● External sync signal input

*3 When switch S1 is set to "*E", -9 V is sent from the output pin of S1. Therefore, IC8 is turned on, and IC9 is turned off. The external sync signal input mode is then selected.
To obtain external sync operation, the two signals below can be input as an external sync signal input.
①HDI/VD signal
②VS or sync signal

*3 [In case the board suffix -11 and -12 of SG-199P board]
When switch S1 is set to EXT, -9 V is sent from the output pin of S1. Therefore, IC6 and IC8 are turned on, and IC7 and IC9 are turned off. The external sync signal input mode is then selected.

① HD/VD signal sync mode
To operate a camera in the HD/VD signal sync mode, HD and VD signals are input from the connector on the rear panel. The input enable signal levels of the HD and VD signals are 2 to 5 Vp - p. The input HD and VD signals are passed through the CN and MB boards and input from pins 5 and 6 of connector CN1.
To terminate the HD and VD signals input from the outside in 75 ohms, switches S2 and S3 for external sync signal termination are set to ON. Switch S2 corresponds to the HD signal, and switch S3 to the VD signal. To terminate no HD and VD signals in 75 ohms, S2 and S3 are set to OFF.

*4 The HD signals passed through a terminatting circuit is input to an inverter primarily consisting of Q2.

*4 [In case the board suffix -11 and -12 of SG-199P board]
The HD signals passed through a terminatting circuit is input through analog switch IC6 to an inverter primarily consisting of Q2.

In the inverter, the negative HD signal is inverted to produce a positive HD signal. The signal level then becomes approximatery 4.5 V. The resultant HD signal is passed through two-stage gate circuit IC3, waveform-shaped, and adjusted to a level of appoximatery 5 Vp-p. The signal is then sent to sync signal generator IC1 in a positive form. The gate in the second stage of gate circuit IC3 functions as aawitch.
When HD and VD signals are not input simultaneously and only the HD signal is input, the unsuitable state is detected and this gate is set to OFF. This gate functions so that the HD signal is not sent.
The VD signal is passed through a terminating circuit and input through analog switch IC8 to a sync signal separator primarily consisting of Q1 and Q3. The VD signal level becomes approximately 4 Vp - p. The resultant VD signal is passed through two - stage gate circuit IC3, waveform - shaped, and adjusted to a level of approximately 5 Vp - p. The signal is then sent to sync signal generator IC1 in a negative form.

②VS or SYNC signal sync mode
To operate a camera in the VS or SYNC signal sync mode, a VS or SYNC signal is input from the connector on the rear panel. The input enable signal level is a SYNC signal level of 0.3 Vp - p ± 6 dB. The input VS or SYNC signal is input through the CN and MB boards from pin 6 of connector CN1.
To terminate the VS or SYNC signal input from the outside in 75 ohms, switch S3 for external sync signal termination is set to ON. To terminate no VS or sync signal in 75 ohms, switch S3 is set to OFF.
The VS or SYNC signal passed through a terminating circuit is input through analog switch IC8 to a sync signal separator primarily consisting of Q1 and Q3. For the VS signal, in this sync signal separator, only a sync signal is separated from the VS signal and sent in a level of approximately 4 Vp - p. The waveform of the SYNC signal remains unchanged. The sync signal is sent in a level of approximately 4 Vp - p. This SYNC signal is passed through two - stage gate circuit IC3, waveform - shaped, and adjusted to a level of approximately 5 Vp - p. The signal is then sent to sync signal generator IC1 in a negative form.

b. Sync signal generation block
A circuit block primarily consisting of IC1 is a sync signal generator. A 14 MHz clock that the timing pulse generator on the MB board outputs is input through pin 7 of connector CN1 to IC1. IC1 produces the sync signals below required for camera operation from this clock.

| | | |
|---|---|---|
| HD | : | Horizontal sync signal |
| VD | : | Vertical sync signal |
| SYNC | : | Composite sync signal |
| BLKG | : | Blanking signal |
| FLD | : | Field identification signal |
| INT/EXT | : | Sync mode selection signal<br>Internal sync mode ····· Low<br>External sync mode ····· High |

IC1 automatically detects internal or external synchronization. If a specific signal is not input to the EXT HD pin and EXT VD pin of IC1 for more than 1024 line cycles, the internal sync mode is entered automatically.
In the normal operating mode in which no special shutter is used, therefore, the internal sync mode is entered if a signal is not input within specified period even if switch S1 is set to EXT.
The information indicating whether the camera's sync mode is internal synchronous or external synchronous is output from IC1 as a sync mode selection signal. In the internal sync mode, a low - level signal is output through pin 9 of connector CN1 from IC1 to the MB board so as to select an oscillator that generates a clock. In the external sync mode, a high - level signal is output in the same way as the above.
A spike filter consisting of D1, C4, R17, and R19 is provided in the output stage so that a BLKG signal exerts no bad influence on the definition of the video signal.

c. Function set block

Sync signal generator IC1 has various functions. These functions can be set by inputting a high- or low-level voltage to the specific input pin according to the mode to be set.

This camera has jumper lands (JR1 through JR9) for setting these functions. Each function can be set by setting the jumper lands to OPEN or SHORT according to the mode to be set.

Jumper lands JR1 through JR9 correspond to the functions below.

JR1 through JR6 : Phase advance of external horizontal sync signal

JR7 and JR8 : Restart reset/normal mode selection

JR9 : Field invert/normal mode selection

For more details of each function, refer to the corresponding item in section 2 - 5. "OPERATION MODE SETTING".

d. Phase comparsion block

A block primarily consisting of IC2 is a phase comparison block. It receives the H reference and H SEP signals output from IC1 and compares the phase.

In the internal sync mode, the H SEP signal is fixed and output.

The phase comparator is then not activated. In the external sync mode, the signals below are output from IC1 as an H SEP signal as required. In the HD/VD signal sync mode, the horizontal sync signal component of an input signal is directly output. In the VS or SYNC signal sync mode, a horizontal sync component is separated from the input VS or SYNC signal in IC1. The separated signal is then output.

The H reference signal is produced from the HD signal generated in IC1. IC1 produces an HD signal from the clock signal input from the MB board. A signal whose phase is delayed relative to this HD signal proportionally to the time specified by the function setting is output to the H reference signal. Assume the phase relation between the H reference and HD signals with the HD signal as reference. The phase of the H reference signal is delayed relative to that of the HD signal by the set time. Assume the H reference signal as reference. The phase of the H reference signal is advanced relative to that of the HD signal by the set time.

As described above, the H SEP signal is produced from a horizontal sync signal input from the outside. The H reference signal is produced from an internal clock signal. To obtain proper external synchronization, the phase of a camera operation clock must coincide with that of a horizontal sync signal input from the outside. Therefore, IC2 compares the phases of the H SEP and H reference signals from IC1 and judges whether the H reference signal should be advanced or delayed to set the phase difference of these signals to zero ("0"). This result is output as a positive or negative control pulse. This control pulse is input through pin 10 of connector CN1 to the MB board, converted into a DC voltage, and input to the voltage - controlled oscillator (VCO) to control the clock frequency. The phase difference between the H SEP and H reference signals is controlled by this loop so that it is zero ("0") at all times. If the frequency deviation of a sync signal input from the outside is within ± 1 % with respect to the frequency of a reference horizontal sync signal, therefore, the camera can be operated normally.

### 2-6-7. PS-268 Board

The PS-268 board is connected to an MB board via board-to-board connector. Speaking functionally, this board is a DC power generation board. The PS-268 board supplies the DC power required for circuit operation for all the boards via the MB board.

The PS-268 board primarily consists of DC/DC converter PU1. The D/D converter is newly designed to miniaturize the XC-75/73 series and to save the power consumption. Therefore, the D/D converter is designed to satisfy the specifications (dimensions and electrical characteristics etc.) for the XC-75/73 series camera.

To normally operate D/D converter PU1, the reference input voltage of a camera supply voltage is set to Vin = 12.0 V, and the range of a guaranteed operating voltage is set to Vin = 10.5 to 15.0 V. This input supply voltage is passed through the CN and MB boards from the connector on the rear panel and input to pins 1 and 2 of connector CN1 on the PS board. When a proper supply voltage is applied to input voltage pin UNREG IN of a D/D converter, three output voltages (-9 V, +5 V, and +15 V) are obtained from the output pin. The +5 V output voltage branches into two paths on the PS board. One is sent to the dedicated analog system, and the other to the dedicated digital system. In this way, by dividing the +5 V voltage into two parts, the mutual bad influence between the 5 V lines caused by the generation of noise is prevented and the circuit malfunction and the deterioration of signal definition are suppressed. These outputs are supplied to all the boards as a DC power or reference voltage as required. The voltage value suitable for each application is used.

However, the three voltage values output from the D/D converter may be insufficient for the performance of some circuits or other voltage values may have to be supplied to some circuits. Some boards thus mount a voltage regulator circuit as required. The PS board mounts a regulator circuit primarily consisting of Q101 and Q102 that produces a -5 V voltage from the -9 V output. The regulator circuit supplies a -5 V voltage to the video signal drive circuit on the MB board. The video signal drive circuit drives the video output of a camera. The -5 V power produced on the PS board is used exclusively for the video signal drive circuit.

### 2-6-8. CN-649 Board

The CN-649 board is a sub-board mounted on the rear panel and is connected to an MB board via flexible board. The CN-649 board mounts a 12-pin multiconnector, 6-pin connector, BNC connector, gain select switch, and manual gain volume control. The CN board primarily functions as a relay board between the external input/output connectors, gain select switch, and volume control, and the MB board.

Each operation is described below for every function.

a. Input/output connectors

CN1 is a 12-pin multiconnector. This connector has a DC IN pin. A DC power (+12 V) required for camera operation is supplied from this pin. The power input to the CN board is immediately passed through fuse F1. Consequently, this fuse is gone when abnormal power is supplied. This can prevent the main body of a camera from damage. The DC power is sent from the CN board to the PS board via the MB board, then converted into the DC power required for camera operation.

By supplying a proper power, a video output signal is sent from the MB board to the CN board. The video output signal input to the CN board is passed through a 14 MHz trap circuit to eliminate the noise of a 14 MHz component generated by a clock. The resultant signal is output from pin 4 of connector CN1 and BNC connector CN3.

CN1 has an HD signal pin (pin 6) and VD/SYNC signal pin (pin 7). The input/output setting of these pins varies depending on the sync mode.

By connecting a sync signal generator to a camera and inputting an external sync signal, the camera can be operated with external synchronization. During external synchronization, the signals shown in the table below are input from pins 6 and 7 of connector CN1 according to the desired external sync mode.

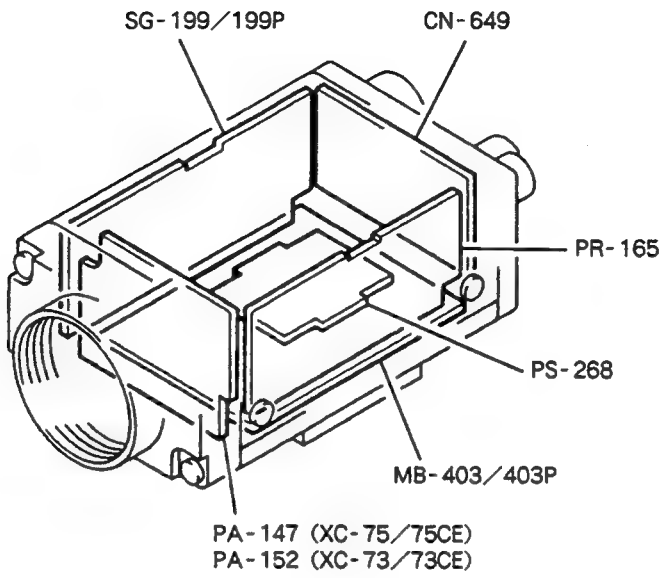
| Pin No. | External synchronization mode | | |
|---|---|---|---|
| | HD/VD | VS or SYNC | Restart/reset |
| 6 | HD signal | ——— | HD signal |
| 7 | VD signal | VS or SYNC signal | Signal reset |

During internal synchronization, HD and VD signals can be output from pins 6 and 7 of connector CN1 using a switch on the SG board.
A clock signal can be also output from CN1. Jumper land JR1 on the CN board is usually set to OPEN. A clock signal is output from pin 9 of connector CN1 by setting jumper land JR1 to SHORT. CN2 is a 6-pin connector. Generally, this connector is connected to an auto iris lens.
The video signal for the auto iris lens output from the PR board is input through the MB board to the CN board and output through a low-pass filter from pin 5 of connector CN2. The iris of the auto iris lens is automatically adjusted using this signal. The power (+12 VDC) for the auto iris lens is output from pin 6 of connector CN2.
CN2 also has the pins below for special application.
Pin 1 is a field identification signal output pin. When the camera operates in the noninterlace mode, a high-level signal is output from the SG board as a field identification signal during odd field scanning. A low-level signal is also output from the SG board during even field scanning. This signal is input from the SG board to the CN board via the MB board and output through a low-pass filter from pin 1 of connector CN2.
Pin 2 is a trigger signal input pin. To control the timing of an exposure start from the outside during special electronic shutter setting, a trigger signal is input from this pin.
For more details of the input signal condition and shutter operation, refer to the corresponding item in section 2-5. "OPERATION MODE SETTING".

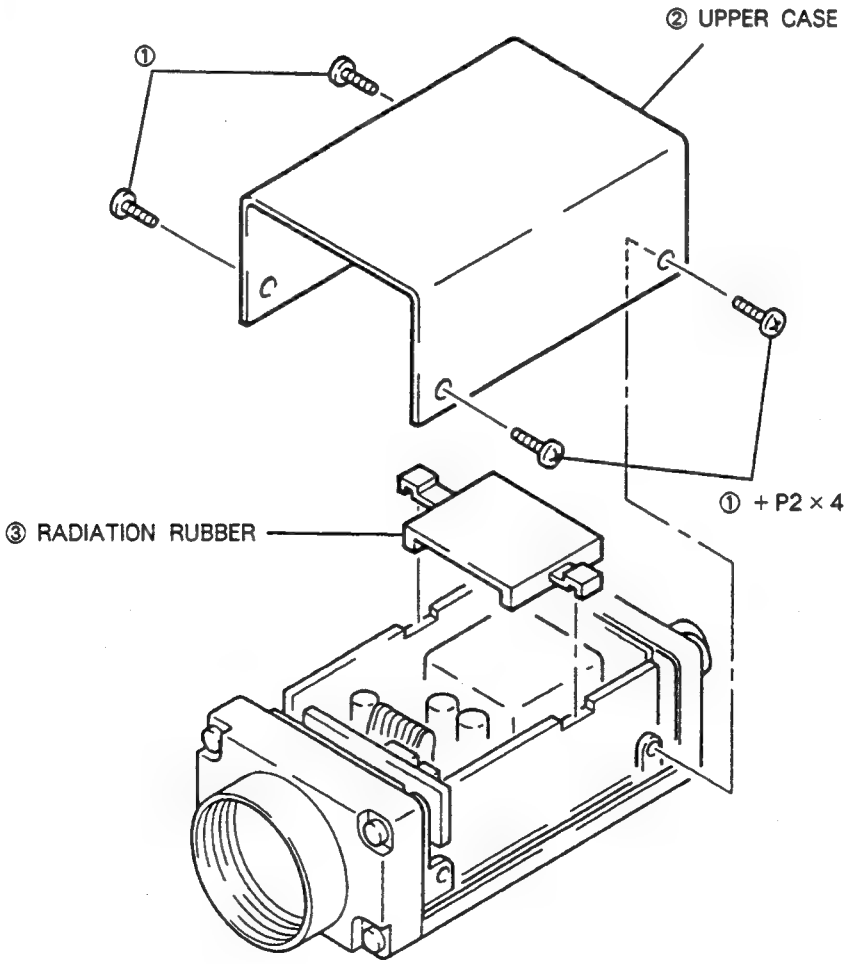
b. Gain select switch and volume control
S1 is a gain select switch. The gain of a video output signal is set using this switch.
AGC (automatic adjustment), FIX (fixed), and MANU (manual adjustment) modes are available for the gain setting. The desired mode is selected using this switch.
S1 has two output pins. A high- or low-level voltage is selected using S1 in accordance with the mode to be set and output as a control voltage. This control voltage is designed so that the combination of two output levels differs for every set mode. Therefore, the PR board that receives this voltage can judge the gain mode by the control voltage sent from the CN board via the MB board. The control voltage is input to the analog switch on the PR board as a control signal to select a switch so that the camera operates in the set gain mode.
In the MANU (manual adjustment) gain mode, the gain of the camera can be manually adjusted to the desired gain in the range of 0 dB to +18 dB using manual gain volume control RV1. The voltage value corresponding to the desired gain is output from the CN board using RV1 and sent through the MB board to the signal generator on the PR board to control the gain of a video signal amplifier.
For more details of the gain setting, refer to the corresponding item in section 2 - 5. "OPERATION MODE SETTING".

# SECTION 3
# SERVICE INFORMATION

## 3-1. BOARD LAYOUT

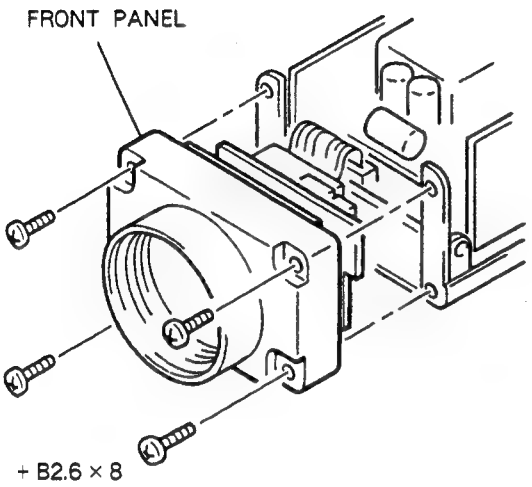



## 3-2. CABINET REMOVAL

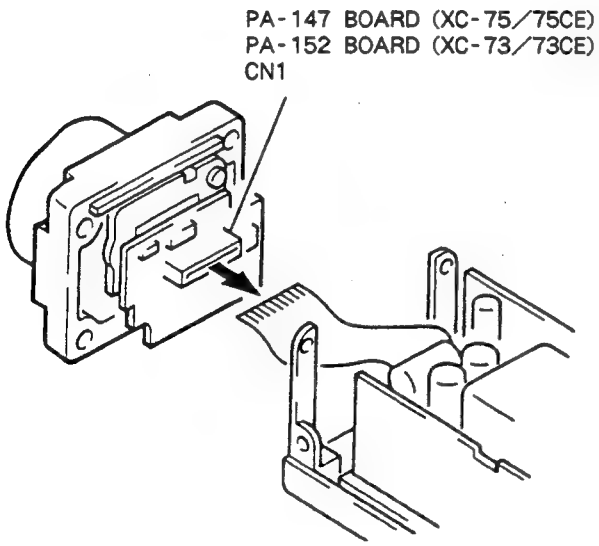


## 3-3. REPLACEMENT OF CCD UNIT

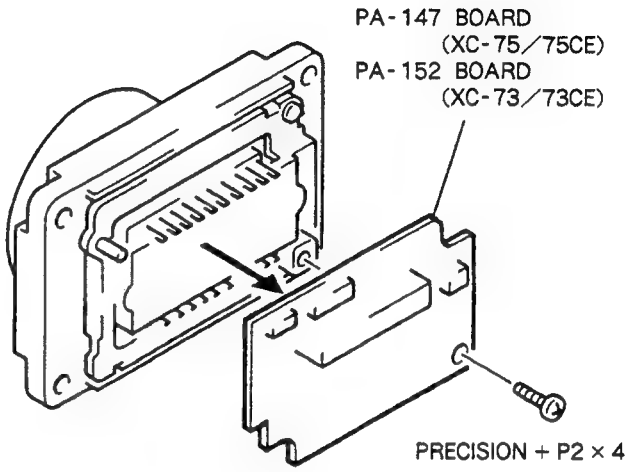
1. Remove the upper case referring to Section 3 - 2 "CABINET REMOVAL".
2. Remove the four screws (+B2.6 × 8) securing the front panel to the chassis.




3. Disconnect the connector CN1 on the PA board.




4. Remove the screw (PRECISION +P2× 4) and unsolder the PA board.

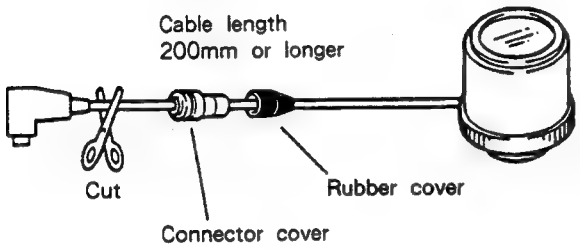



5. Replace the CCD UNIT with a new one. Assemble the unit by reversing the above procedures.
6. After the replacement of CCD UNIT is finished, be sure to perform adjustment, referring to the Section 4 "ALIGNMENT".

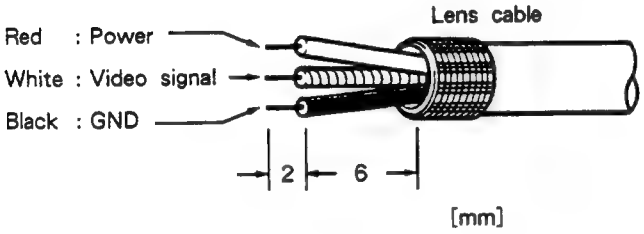
## 3-4. MODIFICATION OF AUTO-IRIS LENS

- Auto-Iris Lens: VCL-16Y
- 6-pin connector: PC-XC06

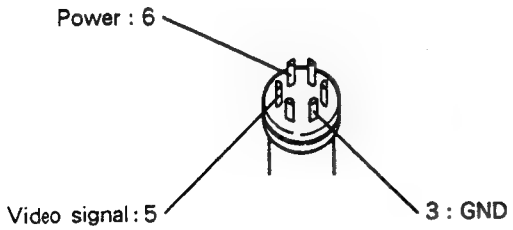
1. Cut the cable of the Auto-Iris Lens VCL-16Y so that the cable length is 200mm or longer. Thread the rubber cover and connector cover of the 6-pin connector PC-XC06 onto the cable.



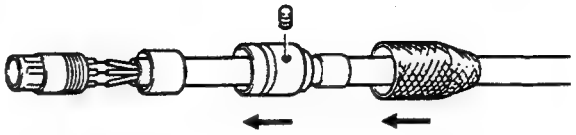

2. Perform the preparation on the inner wires of the lens cable for soldering. There are 6 inner wires (red, white and black) and cut off 3 other wires. Turn back the meshed wires.




3. Connect the 3 inner wires by soldering to the 3-pins of the 6-pin connector.

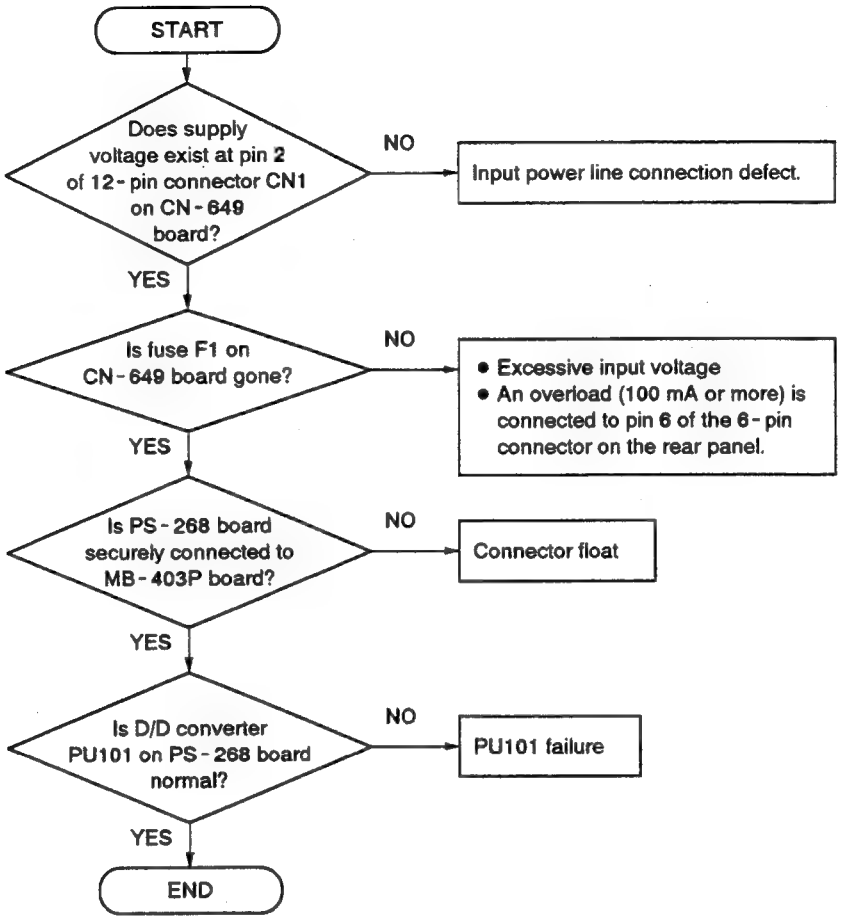



4. Wrap the turned back portion of the meshed wires with the grounding piece provided with the 6-pin connector. Slide the connector cover to cover the connected portion and fix it with the locking screw, then slide the rubber cover to cover the connector cover.

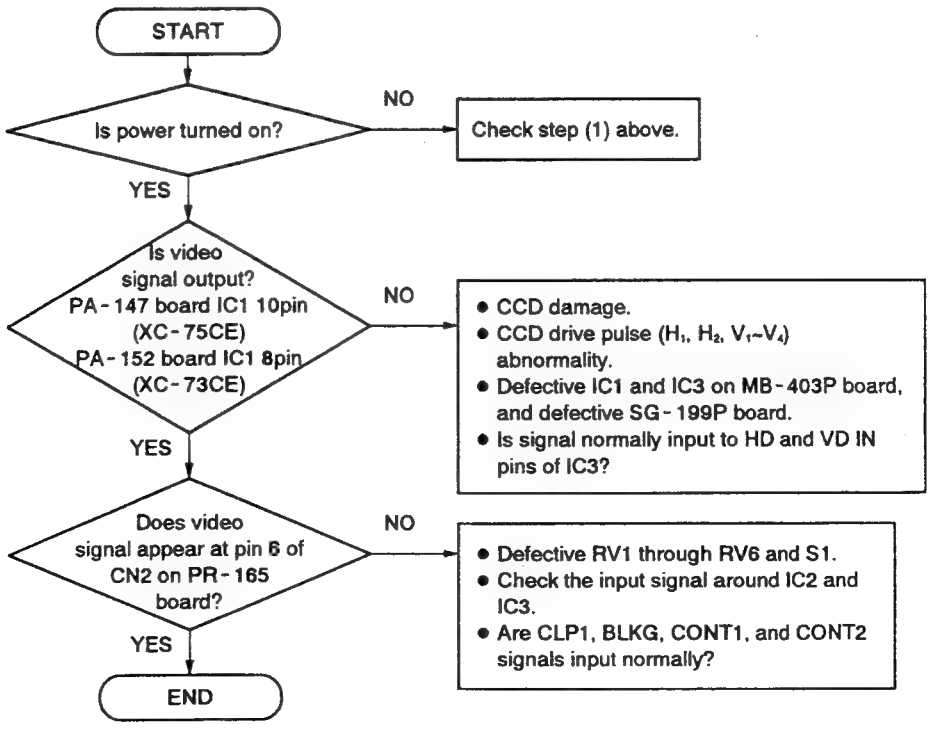


## 3-5. TROUBLESHOOTING

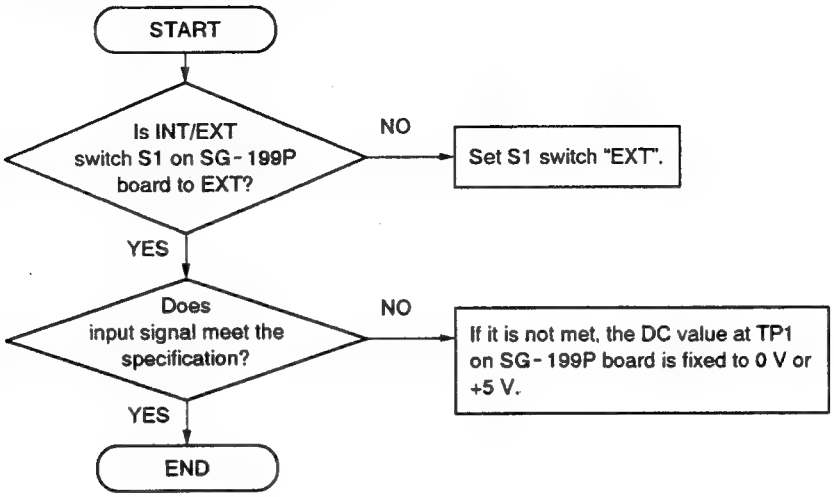
### (1) Power is not turned on.



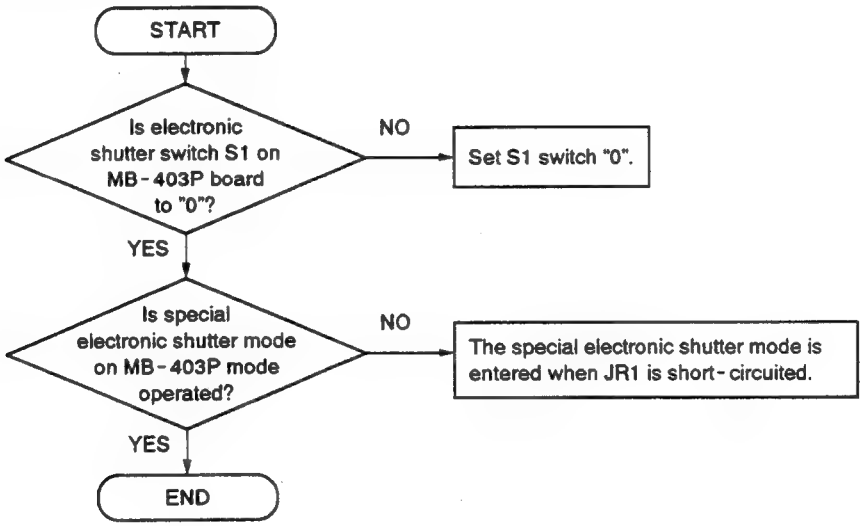

### (2) No display appears.



(3) No external synchronization is established.




(4) Output display is dark excessively.

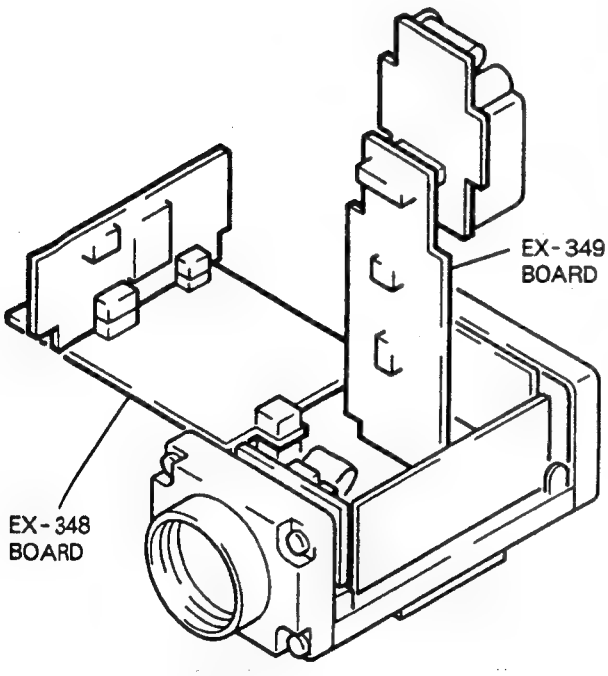


# SECTION 4
# ALIGNMENT

## 4-1. PREPARATION

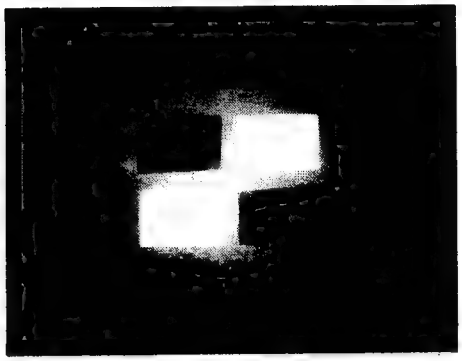
### 4-1-1. Equipment Required

- Oscilloscope
- Waveform monitor
- Black-and-white monitor
- Digital voltmeter
- Power supply unit
- Junction box JB-77(commercially available)and regulated power
- Am meter
- HD/VD signal generator(TG-7(Shibasoku))
- Frequency counter
- Tripod attachment VCT-37(Commercially available)
- Lens standard VCL-12YM
  (Commercially available)(XC-75CE)
  VCL-08YM
  (Commercially available)(XC-73CE)
- Pattern box PTB-500 or PTM-100
  Sony part No. : J-6029-140-A
- Extension board EX-348
  Sony part No. : J-6096-750-A
- Extension board EX-349
  Sony part No. : J-6096-760-A



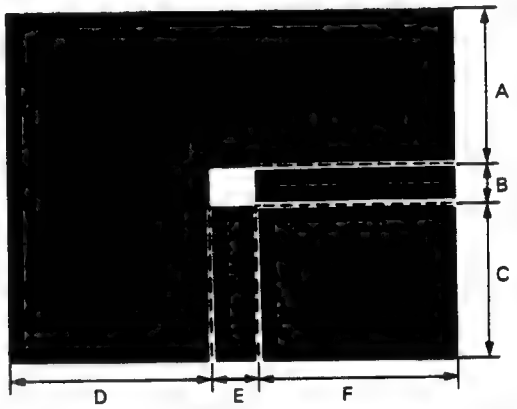

Extention of boards

- Gray scale chart
  Sony part No. : J-6026-130-A



- ND filter(50% transmittance)

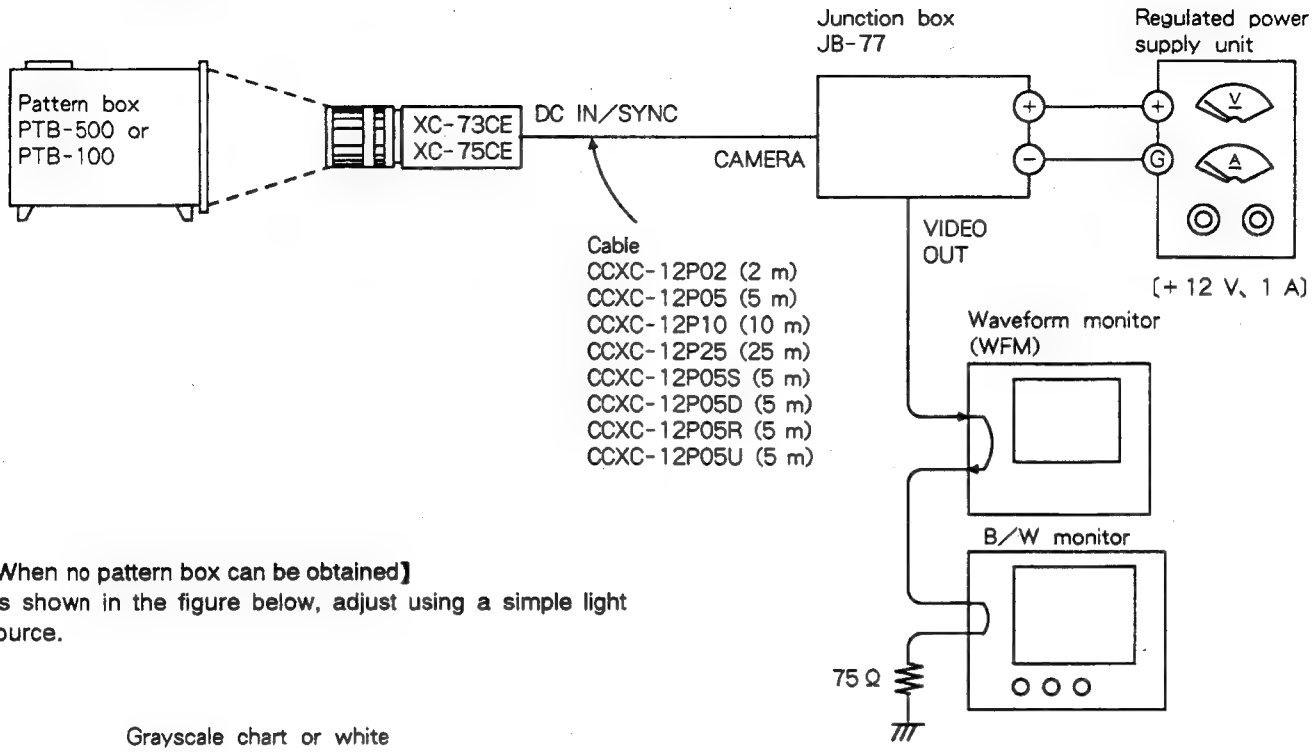
- Window chart
  Make holes on black paper as shown in the following figure. Attach an ND filter having a 10% transmittance to the window.



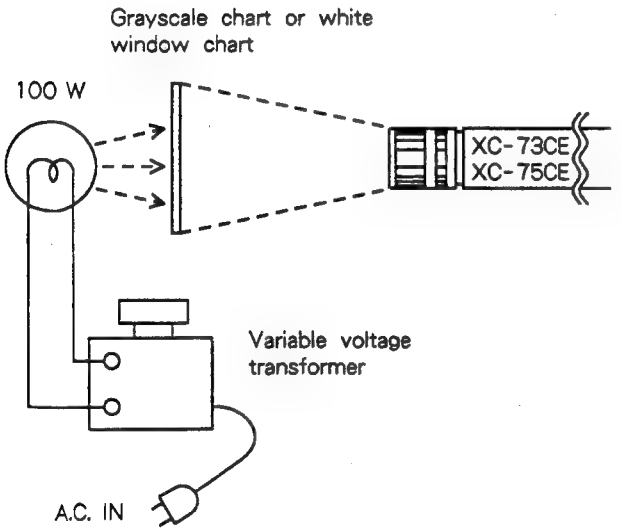

Vertical A:B:C = 4.5:1:4.5
Horizontal D:E:F = 4.5:1:4.5

【When no pattern box can be obtained】
- 100 W electric lamp
- Slidac

### 4-1-2. Connection




【When no pattern box can be obtained】
As shown in the figure below, adjust using a simple light source.




### 4-1-3. Frequency Check for Crystal Oscillator

1. Extend the SG-199P and PS-268 boards using the EX-348/349 extension boards respectively. (See Section 4-1-1. Equipment Required.)
2. Turn the power ON.
3. Connect a frequency counter to Pin 7/Extension board EX-348. Check that the specification A is met.

   A=14.1875 ± 0.001 MHz

4. If the specification is not met, replace C45 on the MB-403P board with one of the following capacitors.

| | | |
|---|---|---|
| C45 | 1pF | 1-162-905-11 |
| | 2pF | 1-162-907-11 |
| | 3pF | 1-162-908-11 |

## 4-2. OVERALL ADJUSTMENT

### Step 1. V RGL and V SUB Voltage Adjustment

**Initial setting:**
Before adjustments set the camera switches as follows.

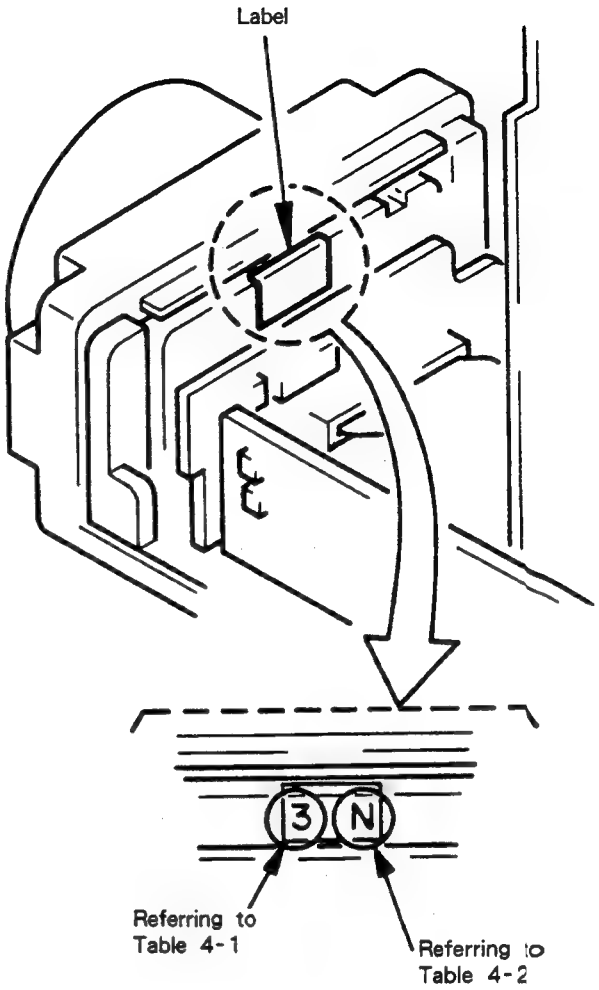
| | |
|---|---|
| S1/SG-199P board | → EXT |
| S2/SG-199P board | → OFF |
| S3/SG-199P board | → OFF |

**Note** : Do not perform this adjustment except when a CCD was replaced. Use a chassis for the ground of a digital voltmeter.

**Measurement equipment** : Digital voltmeter
**Measurement point** : TP1/MB-403P board
TP2/MB-403P board
**Adjustment point** : ⊘ RV1/MB-403P board
⊘ RV2/MB-403P board

**Adjustment procedure** :

1. Check the value of the label attached to the set referring to Tables 4-1 and 4-2, then check the V RGL and V SUB adjustment voltages.
2. Connect a digital voltmeter to TP1 and adjust the value to the V SUB voltage shown in Table 4-2 using ⊘ RV1 on the MB-403P board.
3. Connect a digital voltmeter to TP2 and adjust the value to the V RGL voltage shown in Table 4-1 using ⊘ RV2 on the MB-403P board.




| ① | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| Digit | 1.0 | 1.5 | 2.0 | 2.5 | 3.0 | 3.5 | 4.0 |

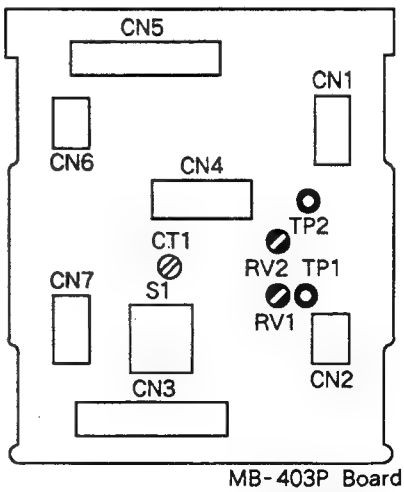
(unit:V)

Table. 4-1:V RGL Voltage

| ② | E | f | G | h | J | K | L |
|---|---|---|---|---|---|---|---|
| Digit | 9.0 | 9.5 | 10.0 | 10.5 | 11.0 | 11.5 | 12.0 |
| ② | m | N | P | Q | R | S | T |
| Digit | 12.5 | 13.0 | 13.5 | 14.0 | 14.5 | 15.0 | 15.5 |
| ② | U | V | W | X | Y | Z | |
| Digit | 16.0 | 16.5 | 17.0 | 17.5 | 18.0 | 18.5 | |

(unit:V)

Table. 4-2:V SUB Voltage




MB-403P Board
– B Side –

### Step 2. VCO Voltage Adjustment

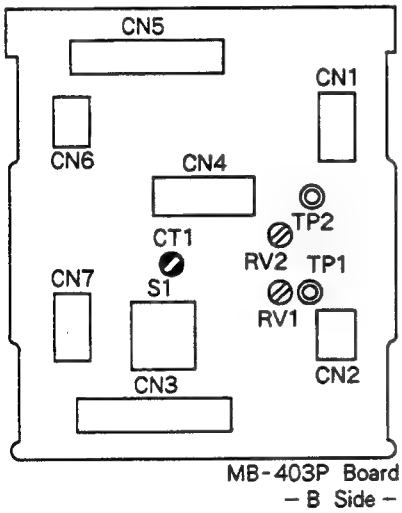
**Measurement equipment :** Digital voltmeter
**Measurement point :** TP1/SG-199P board
**Adjustment point :** ⊘ CT1/MB-403P board
**Specification :** 2.5 ± 0.1 V
**Adjustment procedure :**

1. Input a specified signal to the HD/VD input pin of junction box JB-77 using a signal generator.
2. Adjust ⊘ CT1 on the MB-403P board so that the DC level at TP1 on the SG-199P board is 2.5 ± 0.1 V.
3. Turn off the power switch, remove the extension board, and attach the PS-268 and SG-199P boards directly to the MB-403P board.
4. Turn on the power switch.

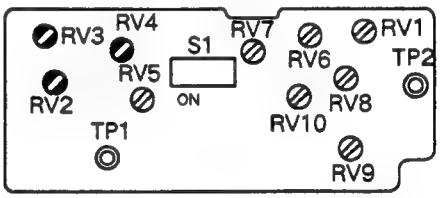
| Input Terminal | HD | VD |
|---|---|---|
| Frequency | 15.625 kHz | 625 fH/2 |

**Note :** The input levels for both VD and HD are $V_{IN}$=2.0~5.0 V p-p

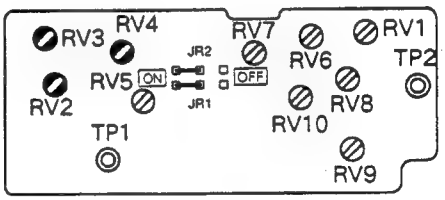
Table. 4-3



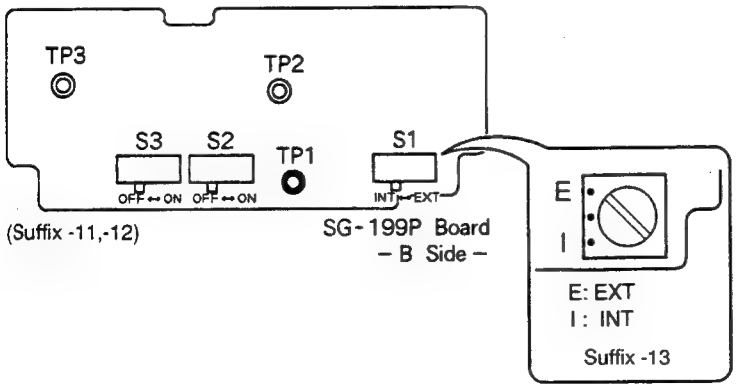
MB-403P Board
– B Side –



(Suffix -11) PR-165 Board
– B Side –



(Suffix -12) PR-165 Board
– B Side –



(Suffix -11,-12) SG-199P Board
– B Side –

### Step 3. Black Tracking Adjustment

**Note :**
Perform step 3, "Black Tracking Adjustment" and step 4, "Pedestal Level Tentative Adjustment" continuously.

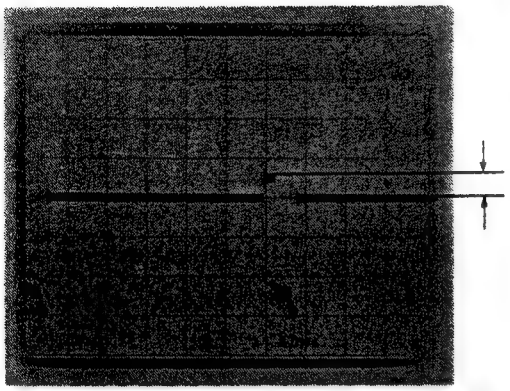
**Measurement equipment :** Oscilloscope
Waveform monitor
**Measurement point :** TP2/PR-165 board
VIDEO OUT pin/rear panel
**Adjustment point :** ⊘ RV2/PR-165 board
⊘ RV3/PR-165 board
⊘ RV4/PR-165 board
**Specification :** Level difference A < ± 2 mV
**Preparation :**

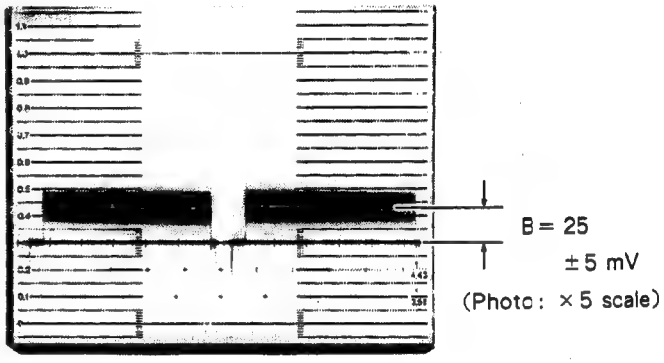
Lens → Closed
GAIN switch/rear panel → M
* S1/PR-165 board (board suffix -11) → ON
* JR1 and JR2/PR-165 board (board suffix -12) → ON

*Above settings are differ due to the board suffix number.

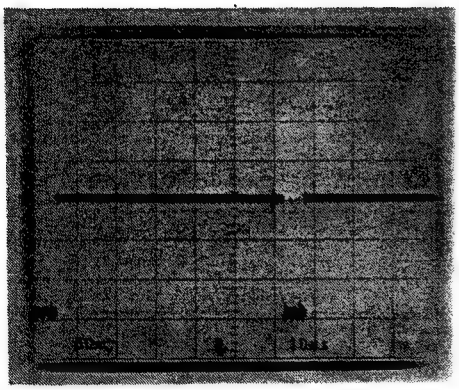
**Adjustment procedure :**

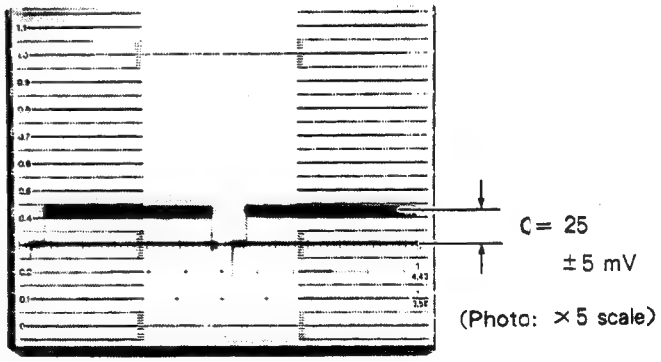
1. Turn the GAIN volume control on the rear panel fully to the right and left and check the waveform using an oscilloscope. Adjust ⊘ RV2 on the PR-165 board so that level difference A is minimum.
2. Set the GAIN switch on the rear panel to F.
3. Turn the GAIN volume control on the rear panel fully to the right and left and adjust ⊘ RV3 on the PR-165 board so that level difference A is minimum.
4. Set the GAIN switch on the rear panel to M.
5. Check the pedestal level of a VIDEO OUT signal using a waveform monitor and adjust ⊘ RV4 on the PR-165 board so that the pedestal level is 25 ± 5mV. (The change in a level is easy to read when the waveform monitor is set to SCALE × 5.)
6. Turn the GAIN volume control on the rear panel fully to the right and left and adjust ⊘ RV2 on the PR-165 board so that the fluctuation in the pedestal level of a VIDEO OUT signal is minimum.
7. Set the GAIN volume control on the rear panel to MINIMUM(turn it counterclockwise).




(GAIN : MAX)






(GAIN : MINIMUM)

B-C : MINIMUM

### Step 4. Pedestal Tentative Adjustment

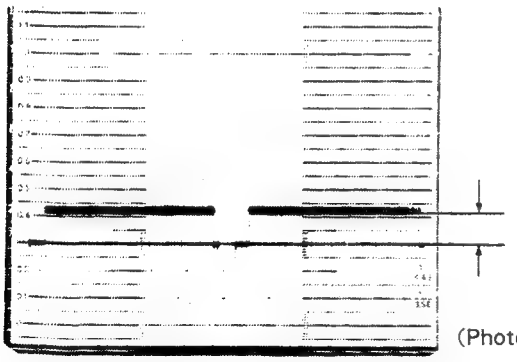
**Note :**
Perform step 3, "Black Tracking Adjustment" before performing this adjustment.

**Measurement equipment :** Waveform monitor
**Measurement point :** VIDEO OUT pin/rear panel
**Adjustment point :** ⊘ RV1/PR-165 board
⊘ RV3/PR-165 board
⊘ RV4/PR-165 board
**Specification :** Level difference A = 25 ± 5mV
**Preparation :**
Lens → Closed
GAIN switch/rear panel → M
* S1/PR-165 board (board suffix -11) → ON
* JR1 and JR2/PR-165 board (board suffix -12) → ON

*Above settings are differ due to the board suffix number.

**Adjustment procedure :**
(The change in a level is easy to read when the waveform monitor is set to SCALE × 5.)

1. Adjust ⊘ RV4 on the PR-165 board so that A = 25 ± 5mV shown in the figure below is obtained.
2. Set the GAIN switch on the rear panel to F.
3. Adjust ⊘ RV3 on the PR-165 board so that A = 25 ± 5mV shown in the figure below is obtained.
4. Set the GAIN switch on the rear panel to M.
5. Set switch S1 on the PR-165 board to OFF.
6. Adjust ⊘ RV1 on the PR-165 board so that A = 25 ± 5mV shown in the figure below is obtained.
7. Set the GAIN switch on the rear panel to F.
8. Using a waveform monitor, check that A = 25 ± 5mV shown in the figure below is obtained.



(Photo : × 5 scale)

### Step 5. Reference Input Adjustment

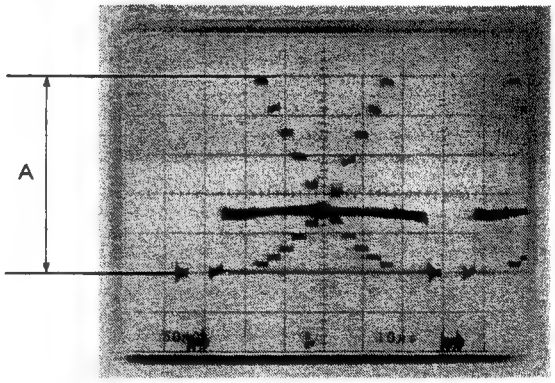
**Measurement equipment :** Oscilloscope
**Object :** Gray scale chartt
**Measurement point :** TP1/PR-165 board
**Adjustment point :** Lens iris
**Preparation :**
* S1/PR-165 board (board suffix -11) → ON
* JR1 and JR2/PR-165 board (board suffix -12) → ON

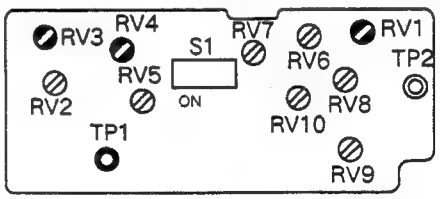
*Above settings are differ due to the board suffix number.

(Check that ⊘ RV5 is set to the position shown below.)

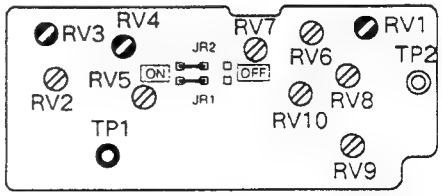

(⊘ RV5 Upper side)

**Specification :** A = 250 ± 10 mV



(Suffix -11) PR-165 Board – B Side –



(Suffix -12) PR-165 Board – B Side –

### Step 6. Video Level Adjustment(1)

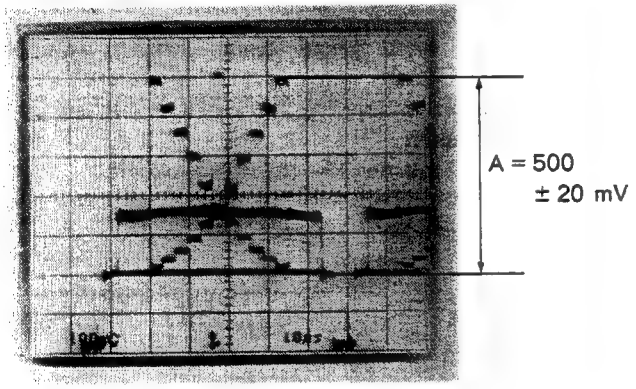
**Measurement equipment :** Oscilloscope
**Object :** Gray scale chart
**Measurement point :** TP2/PR-165 board
**Adjustment point :** ⊘ GAIN volume control/ rear panel

**Preparation :**

GAIN switch/rear panel → M
* S1/PR-165 board (board suffix -11) → ON
* JR1 and JR2/PR-165 board (board suffix -12) → ON

*Above settings are differ due to the board suffix number.

**Specification :** A = 500 ± 20 mV




### Step 7. Video Level Adjustment(2)

**Note :** Perform step 7, "Video Level Adjustment(2)" and step 8, "Sync Level Tentative Adjustment" continuously.

**Measurement equipment :** Waveform monitor
**Object :** Gray scale chart
**Measurement point :** VIDEO OUT pin/rear panel
**Adjustment point :** ⊘ RV6/PR-165 board
⊘ RV7/PR-165 board

**Preparation :**

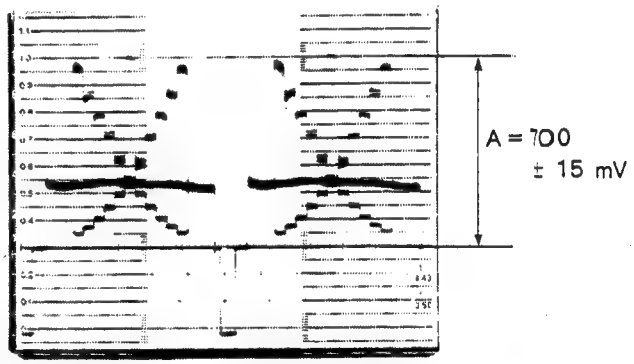
GAIN switch/rear panel → M
* S1/PR-165 board (board suffix -11) → ON
* JR1 and JR2/PR-165 board (board suffix -12) → ON

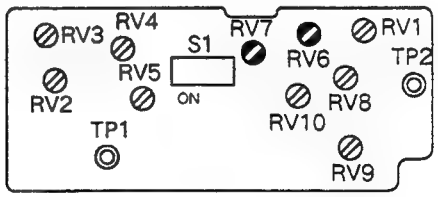
*Above settings are differ due to the board suffix number.

**Specification :** A = 700 ± 15mV

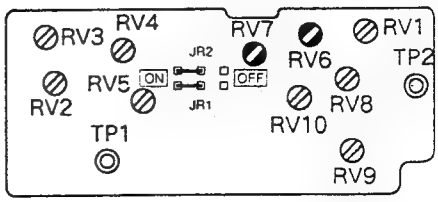
**Adjustment procedure :**

1. Adjust ⊘ RV6 on the PR-165 board so that A = 700 ± 15mV is obtained.
2. Set switch S1 on the PR-165 board to OFF.
3. Adjust ⊘ RV7 on the PR-165 board so that A = 700 ± 15mV is obtained.




(Suffix -11) PR-165 Board – B Side –




(Suffix -12) PR-165 Board – B Side –

### Step 8. Sync Level Adjustment

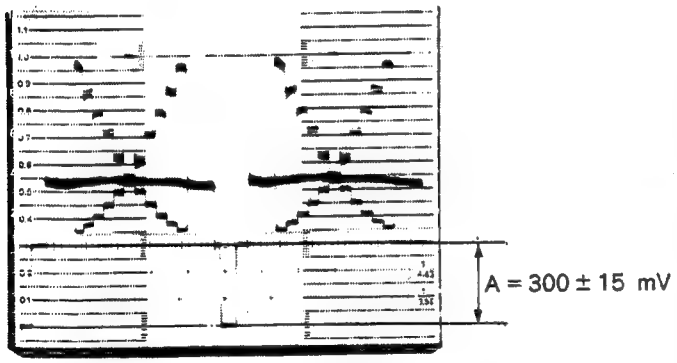
**Note :** Perform step 7, "Video Level Adjustment(2)" before performing this adjustment.
**Measurement equipment :** Waveform monitor
**Object :** Gray scale chart
**Measurement point :** VIDEO OUT pin/rear panel
**Adjustment point :** ◐ RV8/PR-165 board
**Preparation :**

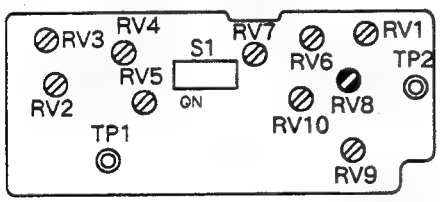
| | |
|---|---|
| GAIN switch/rear panel | → M |
| * S1/PR-165 board (board suffix -11) | → OFF |
| * JR1 and JR2/PR-165 board (board suffix -12) | → OFF |

*Above settings are differ due to the board suffix number.

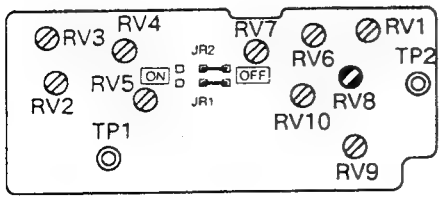
**Specification :** A = 300 ± 15mV

**Adjustment procedure :**
1. Check the sync signal portion of a video output signal using a waveform monitor.
2. Adjust ◐ RV8 on the PR-165 board so that A = 300 ± 15mV is obtained.
3. Perform step 7, "Video Level Adjustment(2)" once again after this adjustment.



(Suffix -11) PR-165 Board – B Side –



(Suffix -12) PR-165 Board – B Side –

### Step 9. Pedestal Adjustment

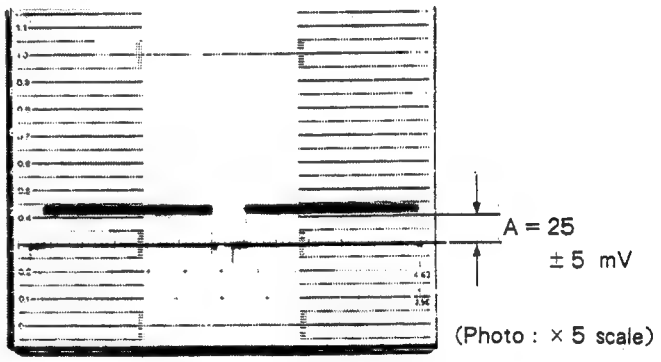
**Measurement equipment :** Waveform monitor
**Measurement point :** VIDEO OUT pin/rear panel
**Adjustment point :** ◐ RV4/PR-165 board
◐ RV1/PR-165 board
**Preparation :**

| | |
|---|---|
| Lens | → Closed |
| GAIN switch/rear panel | → F |
| * S1/PR-165 board (board suffix -11) | → ON |
| * JR1 and JR2/PR-165 board (board suffix -12) | → ON |

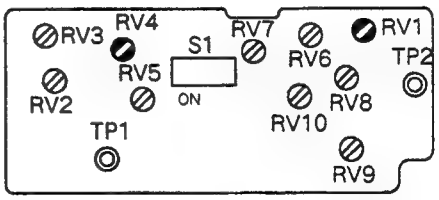
*Above settings are differ due to the board suffix number.

**Specification :** A = 25 ± 5mV

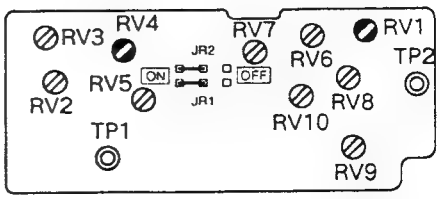
**Adjustment procedure :**
(The change in a level is easy to read when the waveform monitor is set to SCALE × 5.)
1. Check the video output signal using a waveform monitor.
2. Adjust ◐ RV4 on the PR-165 board so that A = 25 ± 5mV is obtained.
3. Set switch S1 on the PR-165 board to OFF.
4. Adjust ◐ RV1 on the PR-165 board so that A = 25 ± 5mV is obtained.



(Photo : × 5 scale)



(Suffix -11) PR-165 Board – B Side –



(Suffix -12) PR-165 Board – B Side –

## Step 10. White Clip Adjustment

**Measurement equipment :** Waveform monitor
**Measurement point :** VIDEO OUT pin/rear panel
**Adjustment point :** ⊘ RV5/PR-165 board
**Preparation :**

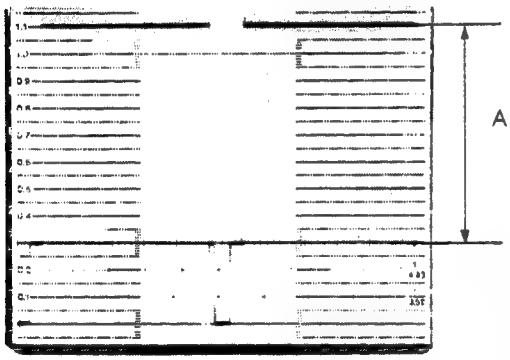
| | |
|---|---|
| Lens | → Open |
| GAIN switch/rear panel | → F |
| * S1/PR-165 board (board suffix -11) | → OFF |
| * JR1 and JR2/PR-165 board (board suffix -12) | → OFF |

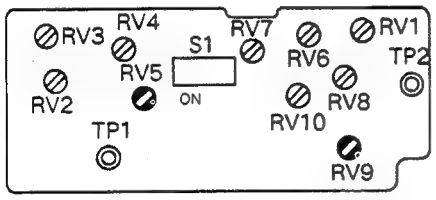
*Above settings are differ due to the board suffix number.

**Specification :** A = 800 ± 20mV

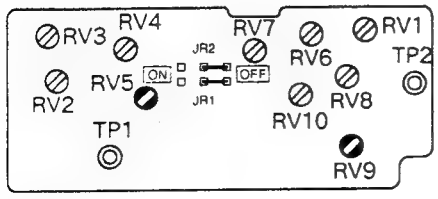
**Adjustment procedure :**

1. Check the video output signal using a waveform monitor.
2. Adjust ⊘ RV5 on the PR-165 board so that A = 800 ± 20mV is obtained.




(Suffix -11) PR-165 Board – B Side –




(Suffix -12) PR-165 Board – B Side –

## Step 11. Automatic Gain Control(AGC)Adjustment

**Measurement equipment :** Oscilloscope
Waveform monitor
**Object :** Gray scale chart (ND filter)
**Measurement point :** VIDEO OUT pin/rear panel
**Adjustment point :** ⊘ RV9/PR-165 board
**Preparation :**

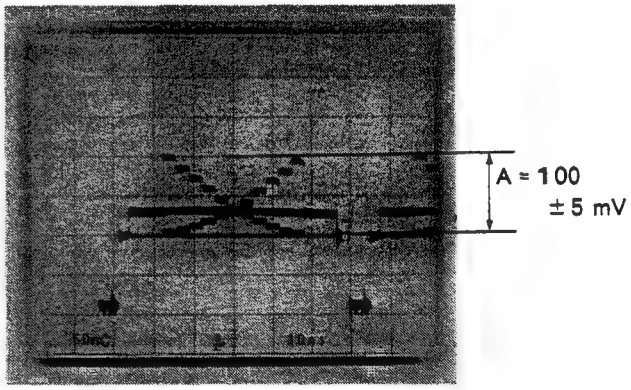
| | |
|---|---|
| GAIN switch/rear panel | → F |
| * S1/PR-165 board (board suffix -11) | → OFF |
| * JR1 and JR2/PR-165 board (board suffix -12) | → OFF |

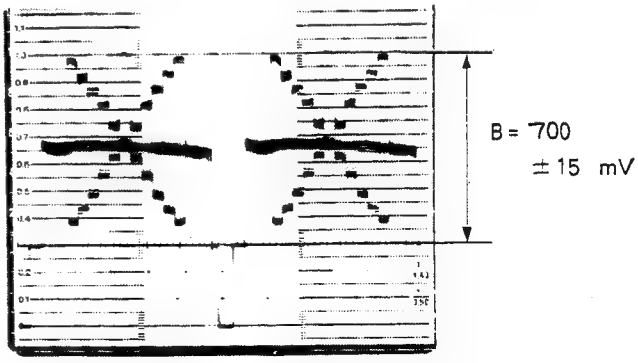
*Above settings are differ due to the board suffix number.

**Specification :** A = 100 ± 5 mV
B = 700 ± 15mV

**Adjustment procedure :**

1. Install the ND filter (50% transmittance) on the lens.
2. Shoot a gray scale chart and check the waveform at TP1 on the PR-165 board.
3. Adjust the lens iris so that A = 100 ± 5 mV is obtained.
4. Check the video output signal using a waveform monitor.
5. Set the GAIN switch on the rear panel to A.
6. Set switch S1 on the PR-165 board to ON.
7. Adjust ⊘ RV9 on the PR-165 board so that B = 700 ± 15mV is obtained.



## Step 12. Maximum Gain Adjustment

**Measurement equipment :** Oscilloscope
Waveform monitor
**Object :** Window chart
**Measurement point :** VIDEO OUT pin/rear panel
**Adjustment point :** ⊘ RV10/PR-165 board
**Preparation :**

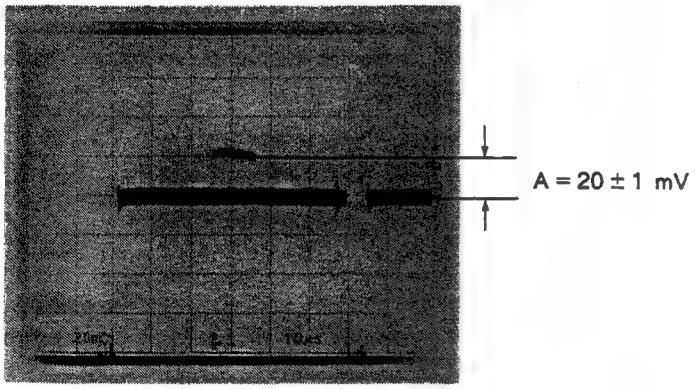
GAIN switch/rear panel → A
* S1/PR-165 board (board suffix -11) → OFF
* JR1 and JR2/PR-165 board (board suffix -12) → OFF

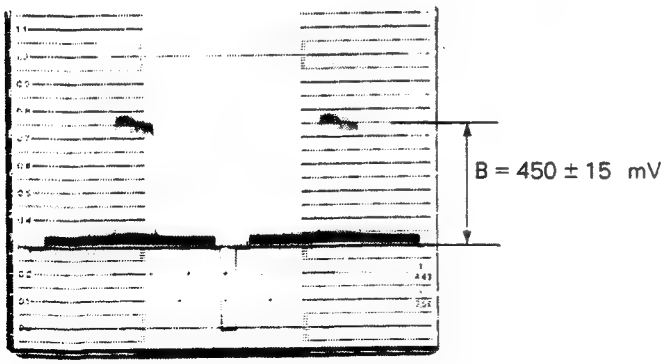
*Above settings are differ due to the board suffix number.

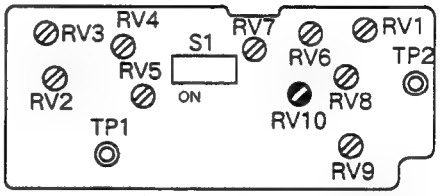
**Specification :** B = 450 ± 15mV

**Adjustment procedure :**

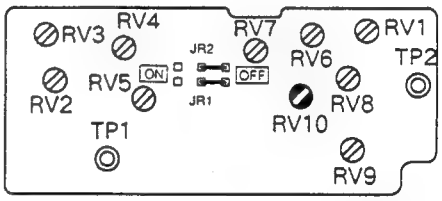
1. Shoot a window chart and check the waveform at TP1 on the PR-165 board.
2. Adjust the lens iris so that A = 20 ± 1 mV is obtained.
3. Check the video output signal using a waveform monitor.
4. Adjust ⊘ RV10 on the PR-165 board so that B = 450 ± 15mV is obtained.




(Suffix -11) PR-165 Board – B Side –




(Suffix -12) PR-165 Board – B Side –

**Note :**

- Set *JR1 and *JR2 on the PR-165 board to ON or OFF position according to user request.
  *In case of board suffix -11, S1 switch is available instead of JR1 and JR2.
- After adjustment is completed, set the camera swiches as follows.

  S2/SG-199P board → ON
  S3/SG-199P board → ON
  GAIN switch/rear panel → F

# 第 1 章
# 取り扱い操作

## 1-1. 概　要

XC-73は固体撮像素子CCD(Charge Coupled Device)を採用した白黒ビデオカメラモジュールです。

### 高画質

768×494画素のCCDにより、きめ細かな画像を再現します。

### 多様なモード設定

用途に応じた多様なモード設定が容易に行えます。例えばゲインについては、外部スイッチの切り換えにより、A (自動調整)、F (固定)、M (手動調整) の選択が可能です。
γについては、*内部ジャンパーの切り換えにより、ON (補正する)、OFF (補正しない) の選択が可能です。
また、内部ジャンパーの配線変更により、電荷の蓄積モードをフレームからフィールドに切り換えれば、ノンインターレースモードの外部同期信号を入力しても、インターレースモードの場合と同一の感度を得ることが可能です。

※ 下記シリアルナンバーのカメラモジュールには、内部ジャンパーの代わりに内部スイッチが付いてます。
XC-73 (UCJ) : 10001-15550

### 外部同期

下記の3種類の入力信号により、カメラモジュールを外部同期で動作させることが可能です。なお、引き込み周波数範囲は、水平周波数の±1%と広くとってあります。

HD、VD信号：入力されたHD、VD信号から、インターレース方式かノンインターレース方式かを自動的に識別し、その方式に応じて外部同期で動作します。

VS (Video、Sync) 信号：VS信号 (映像信号または複合同期信号) により、外部同期で動作します。(HD、VD信号による同期方式とVS信号による同期方式は、外部入力信号に応じて自動的に切り換わります。)

リセットパルス信号：リセットパルス信号により、レジスターの内容を読み出すタイミングを調整できます。

### 内部同期信号出力

FLD信号 (フィールドインデックス信号) は、常時6Pコネクターより出力されています。HD信号とVD信号は、内部スイッチを変更することにより、12Pコネクターから出力させることができます。

### 電子シャッター

FL (フリッカーレス) モードと豊富なシャッタースピード (1/125～1/10000秒) の中から、撮影条件に合った速度が選べます。

### 筐体固定

筐体固定用のネジ穴がCCDの基準面に設けてあります。ここでカメラモジュールを固定すれば、光軸のずれを最小限にとどめることができます。

### XC-77シリーズとの互換性

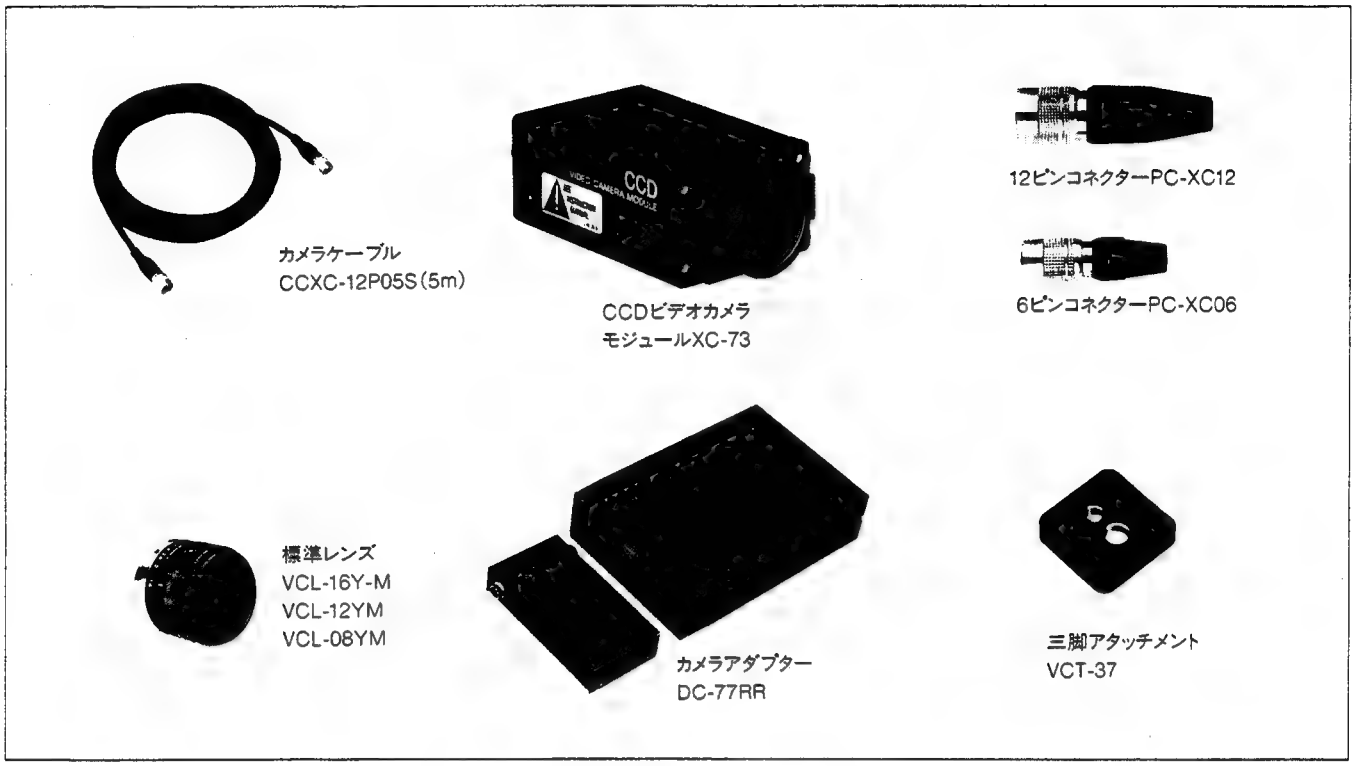
横断面の外形寸法をはじめVIDEO OUT端子の種類や、12ピンコネクターのピン配置もXC-77シリーズと共通していますので、XC-77シリーズのカメラモジュールとそのまま置き換えが可能です。

### その他の特長

- 長寿命　高信頼性
- 画像ひずみが少なく精度の高い画像
- 優れた耐振動衝撃性
- クイックスタート
- 強磁界でも乱れない画像
- 低消費電力 (1.4W)

## 1-2. 構　成

CCDビデオカメラモジュールXC-73を中心としたシステムの構成品目は、次のとおりです。(いずれも別売りです。)




### CCDビデオカメラモジュールXC-73

1/3インチCCDを用いた、小型、高解像度の白黒カメラです。

### 標準レンズVCL-08YM

f=8mm、F1.4の標準レンズで、絞りとピントの調節は手動です。

### カメラケーブルCCXC-12P05S/05D/05R/05U(5m)

カメラモジュール裏面のDC IN/SYNC端子に接続し、電力の供給や映像信号の送出、同期信号の授受を行います。

### 12ピンコネクターPC-XC12

カメラモジュールのDC IN/SYNC端子にカメラケーブルを接続するためのプラグです。

### 6ピンコネクターPC-XC06

オートアイリスレンズを使用する場合に、レンズコードをカメラモジュールのレンズ端子に接続するためのプラグです。

### カメラアダプターDC-77RR

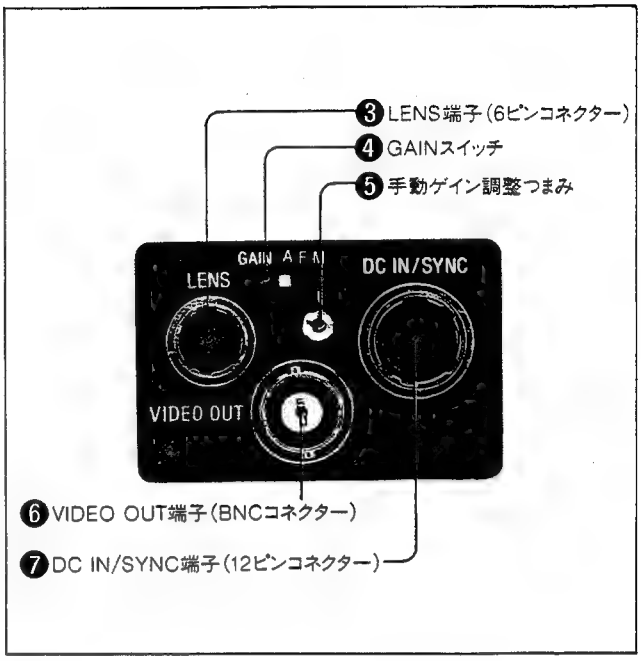
AC電源から電力を供給する場合に、カメラモジュールに接続して使用します。映像信号の送出および同期信号の授受も行えます。

### 三脚アタッチメントVCT-37

三脚を使ってカメラモジュールを固定するとき、このアタッチメントをカメラモジュールの底部に取り付けます。

## 1-3. 各部の名称と使いかた

### CCDビデオカメラモジュールXC-73

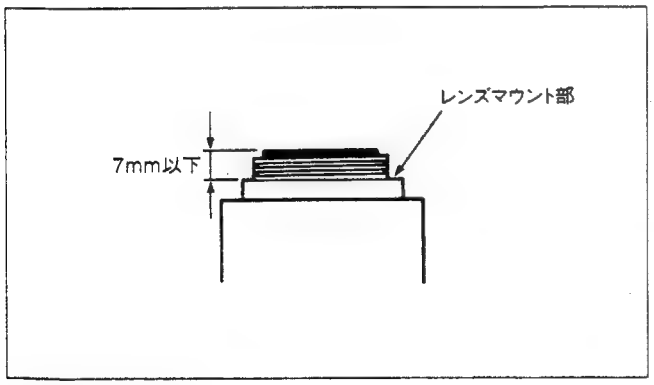




**❶レンズマウント(Cマウント)**

標準レンズVCL-08YMなど、Cマウント式のレンズや光学機器を取り付けます。

**ご注意**

Cマウント式のレンズとして、レンズマウント面からの飛び出し量が7mm以下のものを使用してください。



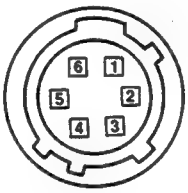

**❷基準穴(底面)**

カメラモジュール固定用に高い精度で切られたネジ穴です。ここでカメラモジュールを固定すると、光軸のずれを最小限にとどめることができます。寸法など詳しくはサービスマニュアルをご覧ください。

**❸LENS(レンズ)端子(6ピンコネクター)**

オートアイリスレンズのプラグを接続すると、レンズの絞りを自動調整することができます。

この端子のピン配置は下図のとおりです。




| ピン番号 | 入出力番号 |
|---|---|
| 1 | FLD信号出力 |
| 2 | トリガー |
| 3 | アース |
| 4 | — |
| 5 | 映像信号出力 |
| 6 | DC+12V |

**❹GAIN (ゲイン)スイッチ**

スイッチの切り換えにより、A(自動調整)、F(固定)、M(手動調整)の各モードが選択できます。

**❺手動ゲイン調整つまみ**

GAIN(ゲイン)スイッチでMを選択した場合、このつまみでゲインを調整できます。

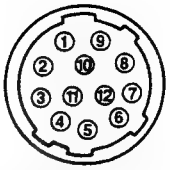
**❻VIDEO OUT(映像出力)端子(BNCコネクター)**

カメラモジュールからの映像信号が出力されます。DC IN/SYNC端子にカメラケーブルCCXC-12P05Sを接続した状態で、DC IN/SYNC端子からの映像出力を75Ωで終端しない場合にのみ、この端子を使用できます。

**❼DC IN/SYNC(DC電源／同期信号入力)端子(12ピンコネクター)**

カメラケーブルCCXC-12P05Sを接続して、DC＋12Vの電力の供給を受けるとともに、カメラモジュールからの映像信号を送出します。また、同期信号発生器を接続して外部同期信号(VSまたはHD/VD信号)を入力すれば、カメラモジュールを外部同期で動作させることができます。

この端子のピン配置は右図のとおりです。




| ピン番号 | 外部同期モード | | | カメラ同期信号出力 |
|---|---|---|---|---|
| | HD/VD | VS | リスタートリセット | |
| 1 | アース | アース | アース | アース |
| 2 | DC＋12V | DC＋12V | DC＋12V | DC＋12V |
| 3 | 映像出力(アース) | 映像出力(アース) | 映像出力(アース) | 映像出力(アース) |
| 4 | 映像出力(信号) | 映像出力(信号) | 映像出力(信号) | 映像出力(信号) |
| 5 | HD入力(アース) | — | HD入力(アース) | HD出力(アース) |
| 6 | HD入力(信号) | — | HD入力(信号) | HD出力*(信号) |
| 7 | VD入力(信号) | VS入力(信号) | リセット(信号) | VD出力*(信号) |
| 8 | — | — | — | クロック出力(アース) |
| 9 | — | — | — | クロック出力**(信号) |
| 10 | アース | アース | — | アース |
| 11 | DC＋12V | DC＋12V | — | DC＋12V |
| 12 | VD入力(アース) | VS入力(アース) | リセット(アース) | VD出力(アース) |

* HD、VD出力を得るには、内部スイッチの変更が必要です。詳しくはサービスマニュアルをご覧ください。

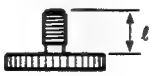
** クロック出力を得るには、内部ジャンパーの配線変更が必要です。詳しくはサービスマニュアルをご覧ください。

## 三脚アタッチメントVCT-37

三脚の取り付け部のネジは次の規格のものを使用してください。

ISO規格　ℓ＝4.5mm±0.2mm

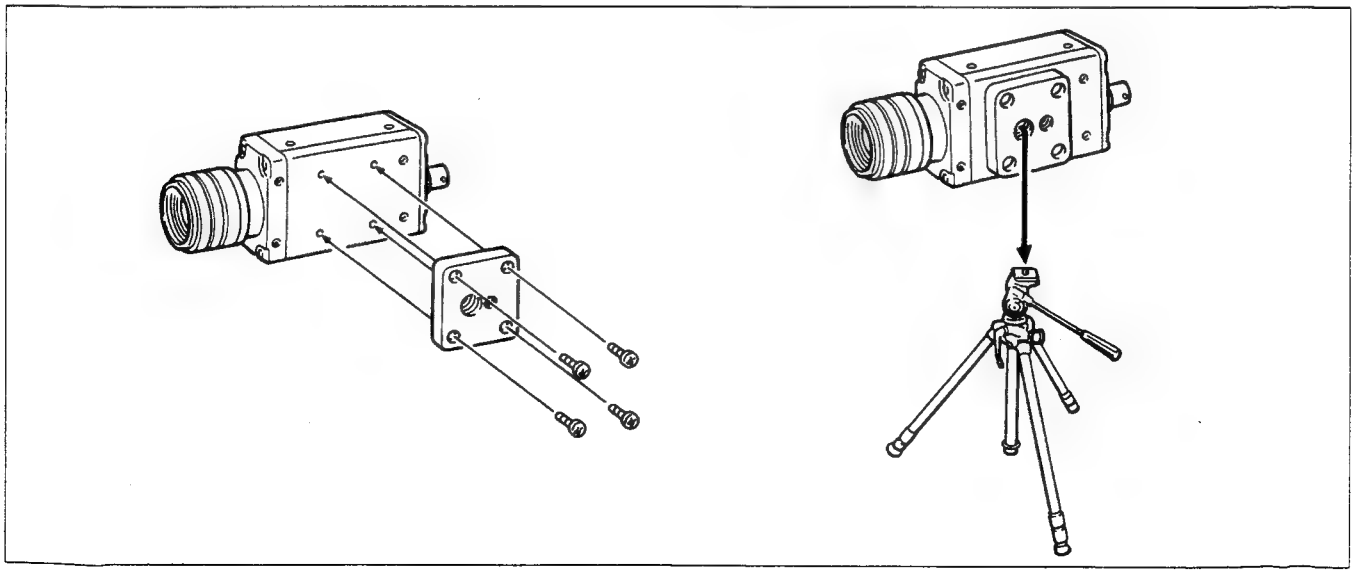
ASA規格　ℓ＝0.197インチ




**ご注意**

三脚アタッチメントをCCDビデオカメラモジュールに取り付けるときは、長さ4mm以内のネジをご使用ください。

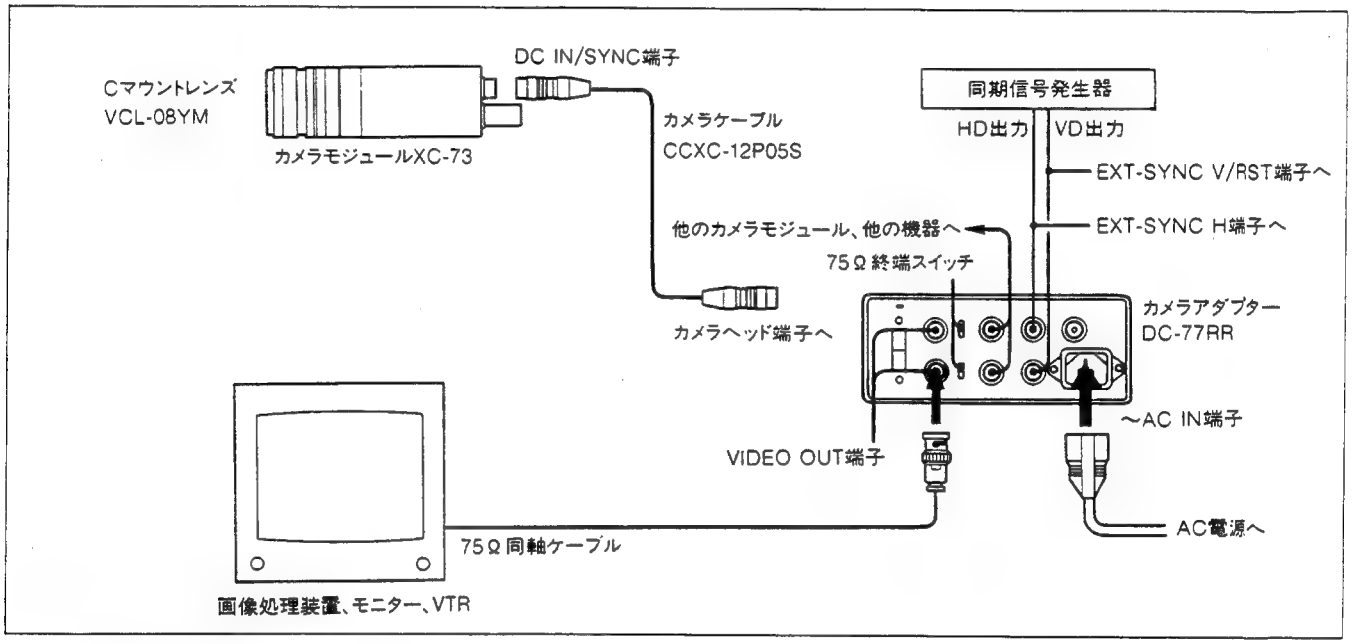
### 取り付けかた



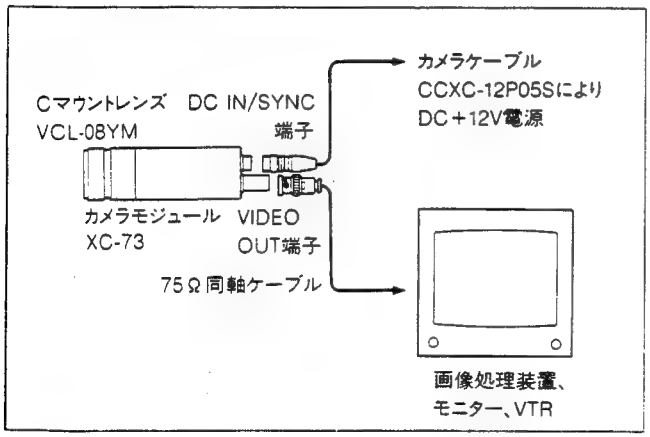
## 1-4. 接続例

### AC電源を使用する場合

カメラモジュールを、AC電源用のアダプターを介して電源に接続します。カメラアダプターDC-77RRの詳細については、専用の取り扱い説明書をご参照ください。




### DC電源に直接接続する場合




**ご注意**

映像出力をVIDEO OUT端子から取り出すときは、DC IN/SYNC端子は電源供給用に使い、DC IN/SYNC端子の接続にはCCXC-12P05Sケーブルをご使用ください。このとき12ピンコネクターの映像出力を終端しないでください。

## 1-5. モードの初期設定

本機では、次の7項目についてそれぞれモードの切り換えが可能です。各項目とも表中□で囲ったモードが、工場出荷時の初期設定モードです。設定モードの変更については、サービスマニュアル及びカメラアダプターDC-77RRの取扱説明書をご覧ください。

| 項目 | モード | 備考 |
|---|---|---|
| ゲイン | A<br>[F]<br>M | ゲイン自動調整<br>ゲイン固定<br>ゲイン手動調整 |
| γ | ON<br>[OFF] | γ補正する<br>γ補正せず |
| 75Ω終端 | [ON]<br>OFF | 終端する<br>終端せず |
| HD/VD信号 | [EXT IN]<br>INT OUT | 外部信号入力<br>内部信号出力 |
| 電子シャッター | [OFF]<br>FL<br>1/125, 1/250, 1/500, 1/1000, 1/2000, 1/4000, 1/10000(秒) | フリッカーレス |
| リスタートリセット | ON<br>[OFF] | フレーム同期する<br>フレーム同期せず |
| 電荷蓄積 | [FRAME]<br>FIELD | フレーム蓄積<br>フィールド蓄積 |

## 1-6. 使用上のご注意

### 電源について

DC+12Vで動作します。リップル、ノイズのない安定した電源をお使いください。

### 異物について

内部に液体をこぼしたり、燃えやすいものや金属類を落とさないでください。そのまま使用すると、火災や感電、故障、事故の原因となります。

### 放熱

内部の温度上昇を避けるため、動作中は布などで包まないでください。

### 使用・保管場所

次のような場所での使用および保管はお避けください。

- 極端に暑い所や寒い所。適正使用温度は0～40°Cです。
- 湿気、ほこりの多い所。
- 雨にあたる所。
- 激しい振動のある所。
- 強力な電波を発生するテレビ、ラジオの送信所の近く。

### お手入れ

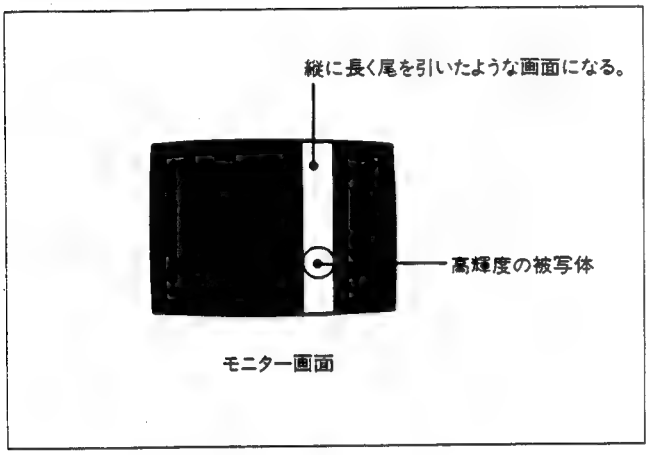
レンズや光学フィルターの表面に付着したごみやほこりは、ブロアーで払ってください。外装の汚れは、乾いた柔らかい布でふきとります。ひどい汚れは、中性洗剤溶液を少し含ませた布でふきとった後、からぶきします。アルコール、ベンジンなどは、変質したり塗料がはげることがありますので、使用しないでください。

## 1-7. CCD 特有の現象

モニター画面上に以下のような現象が現れることがありますが、故障ではありません。

### スミア現象

高輝度の被写体(電灯、蛍光灯、太陽、強い反射光など)を写したときに起こる現象です。




この現象は、CCDがインターライン転送方式を採用しているため、フォトセンサーの深いところに入った赤外線などにより誘起された電荷が、レジスターに転送されるために起こるものです。

### 折り返しひずみ

縞模様、線などを写すと、ギザギザに見えることがあります。

### 傷

CCDはフォトセンサー(素子)が縦横に並んでできており、フォトセンサーのいずれかに欠陥があると、その部分だけ画像が写らず、モニター画面に傷となって見えます(実用上支障がない程度)。

### 微小白点

高温時に暗い被写体を写している場合、画面全体に多数の白点が現れることがあります。

# 第1章
# 取り扱い操作

## 1-1. 概　要

XC-75は固体撮像素子CCD(Charge Coupled Device)を採用した白黒ビデオカメラモジュールです。

### 高画質

768×494画素のCCDにより、きめ細かな画像を再現します。

### 多様なモード設定

用途に応じた多様なモード設定が容易に行えます。例えばゲインについては、外部スイッチの切り換えにより、A (自動調整)、F (固定)、M (手動調整) の選択が可能です。
γについては、*内部ジャンパーの切り換えにより、ON (補正する)、OFF (補正しない) の選択が可能です。
また、内部ジャンパーの配線変更により、電荷の蓄積モードをフレームからフィールドに切り換えれば、ノンインターレースモードの外部同期信号を入力しても、インターレースモードの場合と同一の感度を得ることが可能です。

※ 下記シリアルナンバーのカメラモジュールには、内部ジャンパーの代わりに内部スイッチが付いてます。
XC-75 (UCJ) : 10001-60900

### 外部同期

下記の3種類の入力信号により、カメラモジュールを外部同期で動作させることが可能です。なお、引き込み周波数範囲は、水平周波数の±1%と広くとってあります。

HD、VD信号：入力されたHD、VD信号から、インターレース方式かノンインターレース方式かを自動的に識別し、その方式に応じて外部同期で動作します。

VS (Video、Sync) 信号：VS信号 (映像信号または複合同期信号) により、外部同期で動作します。(HD、VD信号による同期方式とVS信号による同期方式は、外部入力信号に応じて自動的に切り換わります。)

リセットパルス信号：リセットパルス信号により、レジスターの内容を読み出すタイミングを調整できます。

### 内部同期信号出力

FLD信号 (フィールドインデックス信号) は、常時6Pコネクターより出力されています。HD信号とVD信号は、内部スイッチを変更することにより、12Pコネクターから出力させることができます。

### 電子シャッター

FL (フリッカーレス) モードと豊富なシャッタースピード (1/125～1/10000秒) の中から、撮影条件に合った速度が選べます。

### 筐体固定

筐体固定用のネジ穴がCCDの基準面に設けてあります。ここでカメラモジュールを固定すれば、光軸のずれを最小限にとどめることができます。

### XC-77シリーズとの互換性

横断面の外形寸法をはじめVIDEO OUT端子の種類や、12ピンコネクターのピン配置もXC-77シリーズと共通していますので、XC-77シリーズのカメラモジュールとそのまま置き換えが可能です。

### その他の特長

- 長寿命　高信頼性
- 画像ひずみが少なく精度の高い画像
- 優れた耐振動衝撃性
- クイックスタート
- 強磁界でも乱れない画像
- 低消費電力 (1.6W)

## 1-2. 構　成

CCDビデオカメラモジュールXC-75を中心としたシステムの構成品目は、次のとおりです。(いずれも別売りです。)

カメラケーブル
CCXC-12P05S(5m)


CCDビデオカメラ
モジュールXC-75

12ピンコネクターPC-XC12

6ピンコネクターPC-XC06

標準レンズ
VCL-16Y-M
VCL-12YM
VCL-08YM

カメラアダプター
DC-77RR

三脚アタッチメント
VCT-37

### CCDビデオカメラモジュールXC-75

1/2インチCCDを用いた、小型、高解像度の白黒カメラです。

### 標準レンズVCL-12YM

f=12mm、F1.8の標準レンズで、絞りとピントの調節は手動です。

### カメラケーブルCCXC-12P05S/05D/05R/05U(5m)

カメラモジュール裏面のDC IN/SYNC端子に接続し、電力の供給や映像信号の送出、同期信号の授受を行います。

### 12ピンコネクターPC-XC12

カメラモジュールのDC IN/SYNC端子にカメラケーブルを接続するためのプラグです。

### カメラアダプターDC-77RR

AC電源から電力を供給する場合に、カメラモジュールに接続して使用します。映像信号の送出および同期信号の授受も行えます。

### 三脚アタッチメントVCT-37

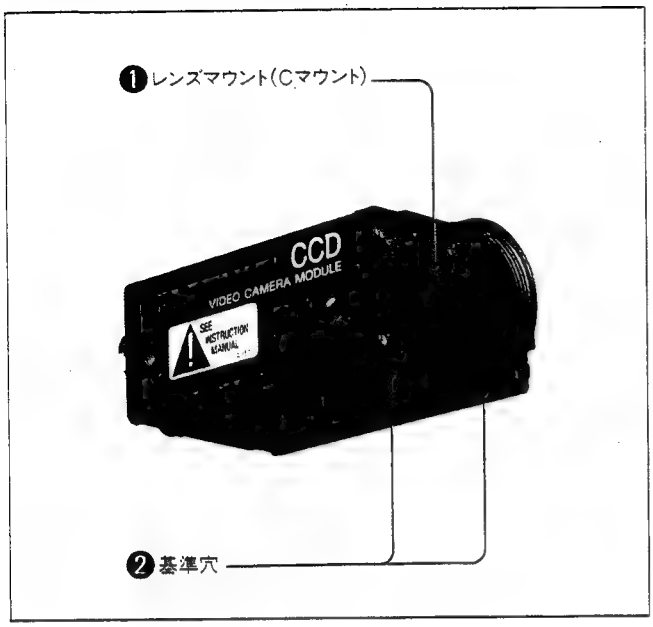
三脚を使ってカメラモジュールを固定するとき、このアタッチメントをカメラモジュールの底部に取り付けます。

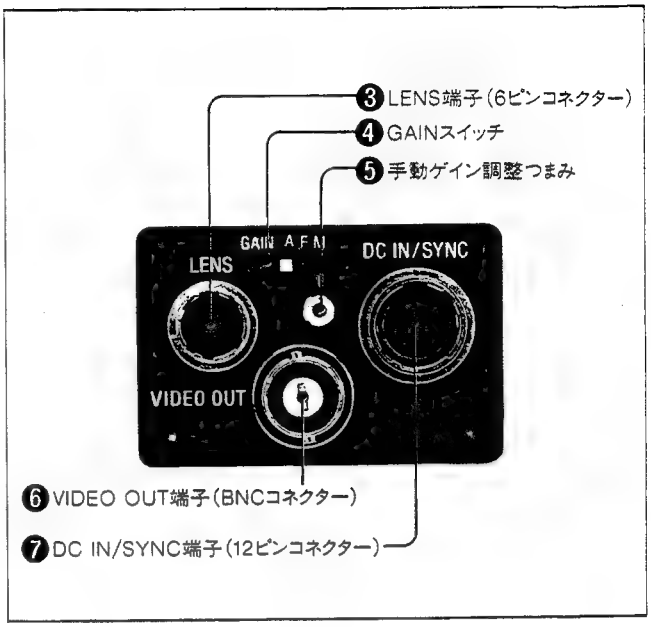
### 6ピンコネクターPC-XC06

オートアイリスレンズを使用する場合に、レンズコードをカメラモジュールのレンズ端子に接続するためのプラグです。

## 1-3. 各部の名称と使いかた

### CCDビデオカメラモジュールXC-75



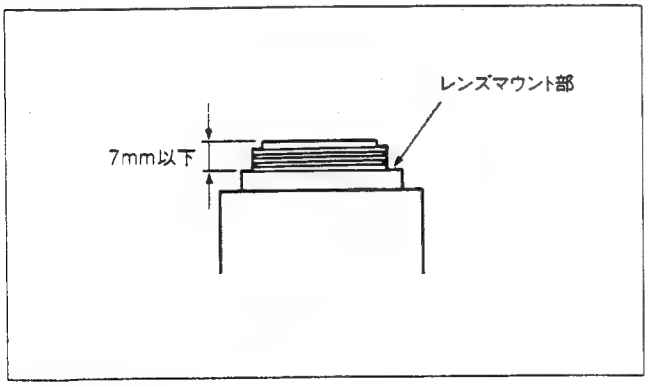




**❶レンズマウント(Cマウント)**

標準レンズVCL-12YMなど、Cマウント式のレンズや光学機器を取り付けます。

**ご注意**

Cマウント式のレンズとして、レンズマウント面からの飛び出し量が7mm以下のものを使用してください。



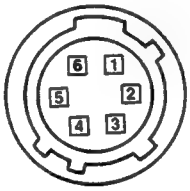

**❷基準穴(底面)**

カメラモジュール固定用に高い精度で切られたネジ穴です。ここでカメラモジュールを固定すると、光軸のずれを最小限にとどめることができます。寸法など詳しくはサービスマニュアルをご覧ください。

**❸LENS(レンズ)端子(6ピンコネクター)**

オートアイリスレンズのプラグを接続すると、レンズの絞りを自動調整することができます。

この端子のピン配置は下図のとおりです。




| ピン番号 | 入出力信号 |
|---|---|
| 1 | FLD信号出力 |
| 2 | トリガー |
| 3 | アース |
| 4 | — |
| 5 | 映像信号出力 |
| 6 | DC+12V |

**❹GAIN (ゲイン)スイッチ**

スイッチの切り換えにより、A(自動調整)、F(固定)、M(手動調整)の各モードが選択できます。

**❺手動ゲイン調整つまみ**

GAIN(ゲイン)スイッチでMを選択した場合、このつまみでゲインを調整できます。

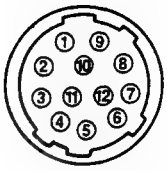
**❻VIDEO OUT(映像出力)端子(BNCコネクター)**

カメラモジュールからの映像信号が出力されます。DC IN/SYNC端子にカメラケーブルCCXC-05Sを接続した状態で、DC IN/SYNC端子からの映像出力を75Ωで終端しない場合にのみ、この端子を使用できます。

**❼DC IN/SYNC(DC電源／同期信号入力)端子(12ピンコネクター)**

カメラケーブルCCXC-12P05Sを接続して、DC+12Vの電力の供給を受けるとともに、カメラモジュールからの映像信号を送出します。また、同期信号発生器を接続して外部同期信号(VSまたはHD/VD信号)を入力すれば、カメラモジュールを外部同期で動作させることができます。

この端子のピン配置は右図のとおりです。




| ピン番号 | 外部同期モード | | | カメラ同期信号出力 |
|---|---|---|---|---|
| | HD/VD | VS | リスタートリセット | |
| 1 | アース | アース | アース | アース |
| 2 | DC+12V | DC+12V | DC+12V | DC+12V |
| 3 | 映像出力(アース) | 映像出力(アース) | 映像出力(アース) | 映像出力(アース) |
| 4 | 映像出力(信号) | 映像出力(信号) | 映像出力(信号) | 映像出力(信号) |
| 5 | HD入力(アース) | — | HD入力(アース) | HD出力(アース) |
| 6 | HD入力(信号) | — | HD入力(信号) | HD出力*(信号) |
| 7 | VD入力(信号) | VS入力(信号) | リセット(信号) | VD出力*(信号) |
| 8 | — | — | — | クロック出力(アース) |
| 9 | — | — | — | クロック出力**(信号) |
| 10 | アース | アース | — | アース |
| 11 | DC+12V | DC+12V | — | DC+12V |
| 12 | VD入力(アース) | VS入力(アース) | リセット(アース) | VD出力(アース) |

* HD、VD出力を得るには、内部スイッチの変更が必要です。詳しくはサービスマニュアルをご覧ください。

** クロック出力を得るには、内部ジャンパーの配線変更が必要です。詳しくはサービスマニュアルをご覧ください。

## 三脚アタッチメントVCT-37

三脚の取り付け部のネジは次の規格のものを使用してください。

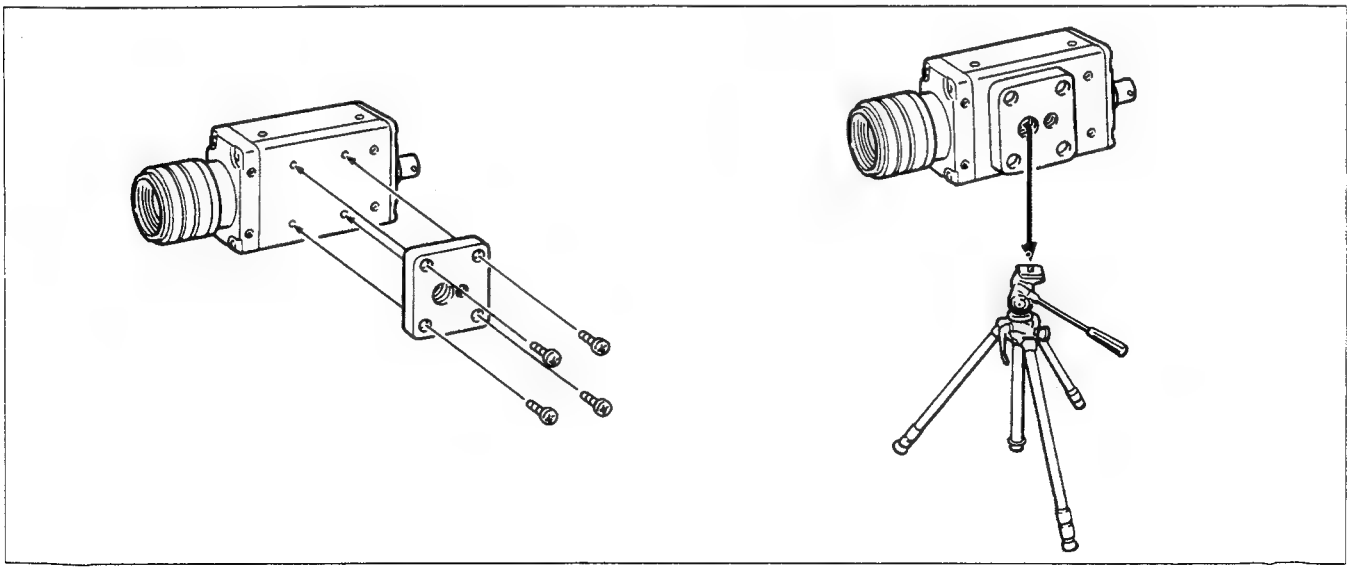
ISO規格　ℓ = 4.5mm ± 0.2mm

ASA規格　ℓ = 0.197インチ


**ご注意**

三脚アタッチメントをCCDビデオカメラモジュールに取り付けるときは、長さ4mm以内のネジをご使用ください。

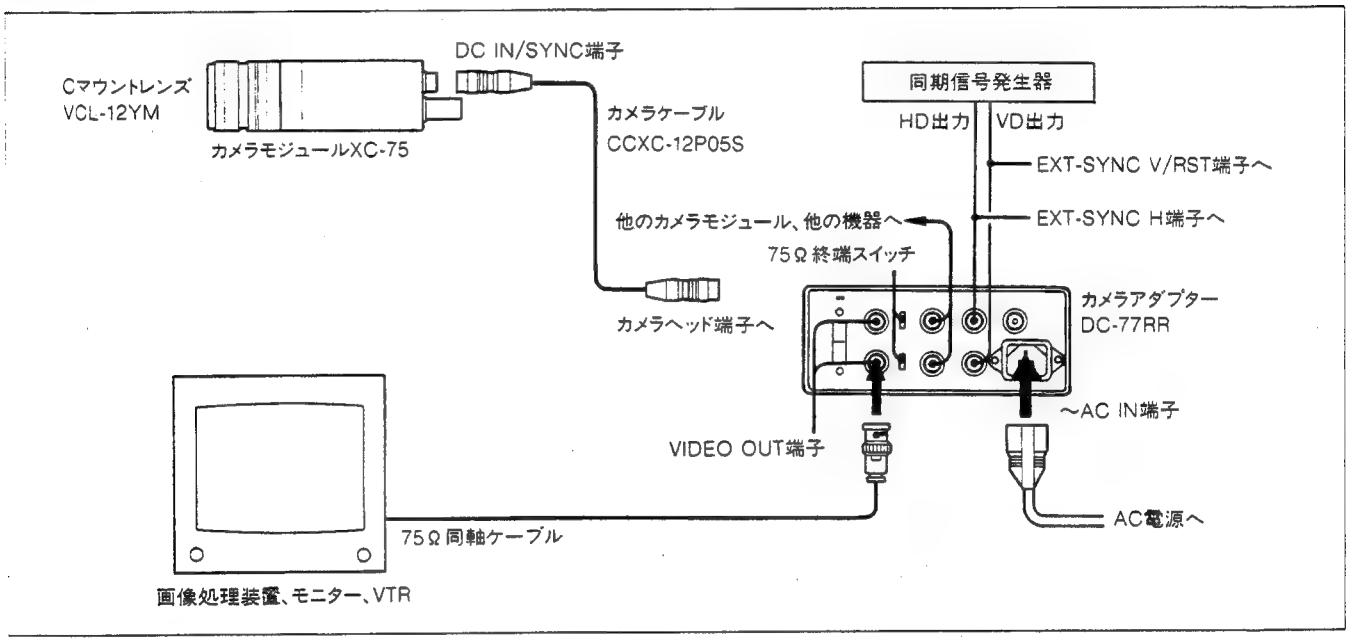
### 取り付けかた



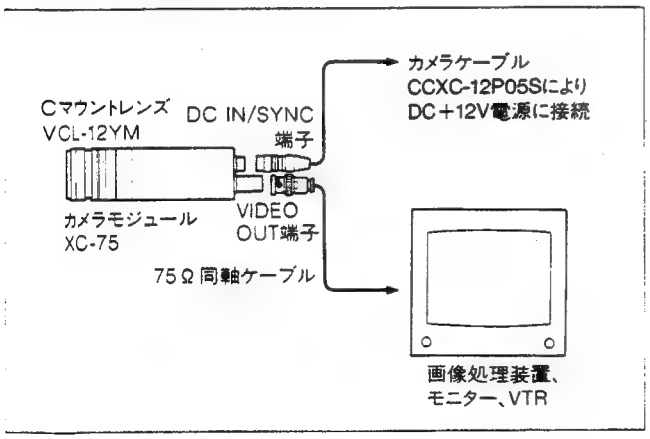
## 1-4. 接続例

### AC電源を使用する場合

カメラモジュールを、AC電源用のアダプターを介して電源に接続します。
カメラアダプターDC-77RRの詳細については、専用の取り扱い説明書をご参照ください。




### DC電源に直接接続する場合




**ご注意**

映像出力をVIDEO OUT端子から取り出すときは、DC IN/SYNC端子は電源供給用に使い、DC IN/SYNC端子の接続にはCCXC-12P05Sケーブルをご使用ください。このとき12ピンコネクター映像出力を終端しないでください。

## 1-5. モードの初期設定

本機では、次の7項目についてそれぞれモードの切り換えが可能です。各項目とも表中□で囲ったモードが、工場出荷時の初期設定モードです。設定モードの変更については、サービスマニュアル及びカメラアダプターDC-77RRの取扱説明書をご覧ください。

| 項目 | モード | 備考 |
|---|---|---|
| ゲイン | A<br>[F]<br>M | ゲイン自動調整<br>ゲイン固定<br>ゲイン手動調整 |
| γ | ON<br>[OFF] | γ補正する<br>γ補正せず |
| 75Ω終端 | [ON]<br>OFF | 終端する<br>終端せず |
| HD/VD信号 | [EXT IN]<br>INT OUT | 外部信号入力<br>内部信号出力 |
| 電子シャッター | [OFF]<br>FL<br>1/125, 1/250, 1/500, 1/1000, 1/2000,1/4000,1/10000(秒) | フリッカーレス |
| リスタートリセット | ON<br>[OFF] | フレーム同期する<br>フレーム同期せず |
| 電荷蓄積 | [FRAME]<br>FIELD | フレーム蓄積<br>フィールド蓄積 |

## 1-6. 使用上のご注意

### 電源について

DC+12Vで動作します。リップル、ノイズのない安定した電源をお使いください。

### 異物について

内部に液体をこぼしたり、燃えやすいものや金属類を落とさないでください。そのまま使用すると、火災や感電、故障、事故の原因となります。

### 放熱

内部の温度上昇を避けるため、動作中は布などで包まないでください。

### 使用・保管場所

次のような場所での使用および保管はお避けください。

- 極端に暑い所や寒い所。適正使用温度は0～40°Cです。
- 湿気、ほこりの多い所。
- 雨にあたる所。
- 激しい振動のある所。
- 強力な電波を発生するテレビ、ラジオの送信所の近く。

### お手入れ

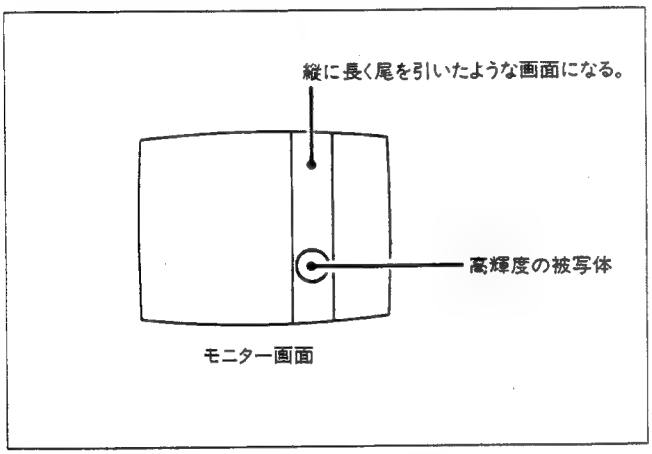
レンズや光学フィルターの表面に付着したごみやほこりは、ブロアーで払ってください。外装の汚れは、乾いた柔らかい布でふきとります。ひどい汚れは、中性洗剤溶液を少し含ませた布でふきとった後、からぶきします。アルコール、ベンジンなどは、変質したり塗料がはげることがありますので、使用しないでください。

## 1-7. CCD特有の現象

モニター画面上に以下のような現象が現れることがありますが、故障ではありません。

### スミア現象

高輝度の被写体(電灯、蛍光灯、太陽、強い反射光など)を写したときに起こる現象です。




この現象は、CCDがインターライン転送方式を採用しているため、フォトセンサーの深いところに入った赤外線などにより誘起された電荷が、レジスターに転送されるために起こるものです。

### 折り返しひずみ

縞模様、線などを写すと、ギザギザに見えることがあります。

### 傷

CCDはフォトセンサー(素子)が縦横に並んでできており、フォトセンサーのいずれかに欠陥があると、その部分だけ画像が写らず、モニター画面に傷となって見えます(実用上支障がない程度)。

### 微小白点

高温時に暗い被写体を写している場合、画面全体に多数の白点が現れることがあります。

# 第2章
# 製品仕様

## 2-1. 仕様（XC-73／75）

### 画像系

| | |
|---|---|
| 撮像素子 | インターライン転送方式CCD |
| 有効画素数 | 768×494（水平／垂直） |
| 撮像面積 | XC-73：1／3インチサイズ |
| | XC-75：1／2インチサイズ |
| 光学黒期間 | 各水平走査線のうち43画素 |
| CCD垂直駆動周波数 | 15.734kHz±1％ |
| CCD水平駆動周波数 | 14.318MHz |
| 信号方式 | EIA方式 |
| セルサイズ | XC-73：6.35×7.4μm（水平／垂直） |
| | XC-75：8.4×9.8μm（水平／垂直） |

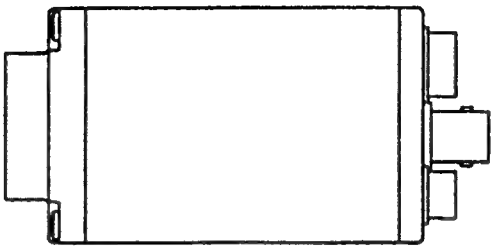
### 光学系、その他

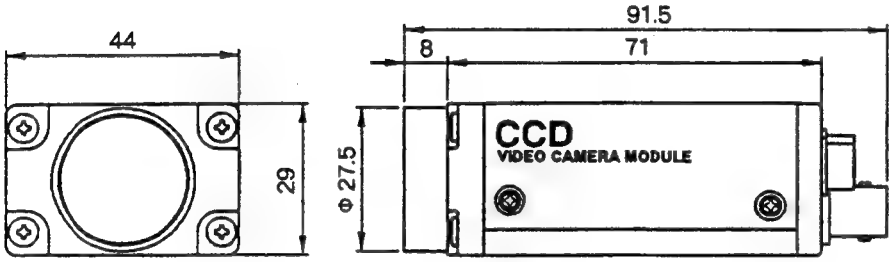
| | |
|---|---|
| レンズマウント | Cマウント |
| フランジバック | 17.526mm |
| 同期方式 | 内部／外部 |
| | （入力信号に応じて自動切り換え） |
| 外部同期入出力 | S、VS（SYNCレベル：0.3$^{+0.3}_{-0.15}$ Vp-p） |
| | HD／VD（HD／VDレベル：2～5Vp-p、入力信号に応じて自動切り換え、入出力の切り換えは内部スイッチによる） |
| 外部同期許容周波数偏差 | |
| | ±1％（水平同期周波数に対して） |
| ジッター | ±50nsec以内 |
| 走査方式 | 525本 |
| | 2：1インタレース／ノンインタレース |
| | （入力信号に応じて切り換え） |
| 映像出力 | 1.0Vp-p、同期負、75Ω不平衡 |
| 水平解像度 | 570TV本（VCL-08YM、開放～F11） |
| 垂直有効ライン数 | 485本（2：1インタレース時） |
| 感度 | 400 lux、F4（γ補正ON、0dB） |
| 最低被写体照度 | 3.0 lux |
| | （自動ゲイン調整時、F1.4、γ補正ON） |
| 映像S／N比 | 56dB |
| ゲイン | 自動ゲイン調整／固定ゲイン／手動ゲイン調整 |
| | （リアパネル上のスイッチで切り換え） |
| γ | γ補正／γ＝1（*内部ジャンパーで切り換え） |
| | ※ 下記シリアルナンバーのカメラモジュールには、内部ジャンパーの代わりに内部スイッチが付いてます。 |
| | XC-73 (UCJ)：10001-15550 |
| | XC-75 (UCJ)：10001-60900 |
| ホワイトクリップ | 115IRE±10IRE |
| 電荷蓄積モード | フレーム／フィールド |
| | （内部ジャンパーの配線変更により切り換え） |
| シャッター機能 | ノーマルシャッター／特殊シャッター |
| | （内部ジャンパーの配線変更により切り換え） |
| シャッタースピード | ノーマルシャッター：フリッカーレス 1/125、1/250、1/500、1/1000、1/2000、1/10000秒（内部スイッチで切り換え） |
| | 特殊シャッター：1/1600～1/100秒 |
| 電源 | DC＋12V（範囲：＋10.5～15V） |
| 消費電力 | XC-73：1.4W |
| | XC-75：1.6W |
| 動作温度 | －5～＋45℃ |
| 保存温度 | －25～＋60℃ |
| 動作湿度 | 20～80％（結露のない状態で） |
| 保存湿度 | 20～95％（結露のない状態で） |
| 耐振動性 | 7G（11Hz～200Hz） |
| 耐衝撃性 | 70G |
| 外形寸法 | 44（W）×29（H）×91.5（D）mm（突起部含む） |
| 質量 | 140g |
| 附属品 | レンズマウントキャップ（1） |
| | 取扱説明書（1） |

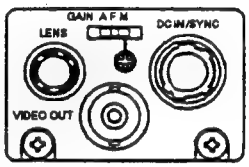
仕様および外観は改良のため予告なく変更することがあり ますが、ご了承ください。

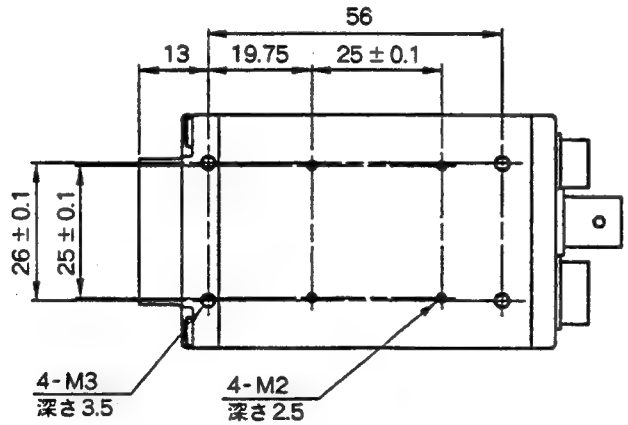
寸法

カメラモジュール〈XC-75〉

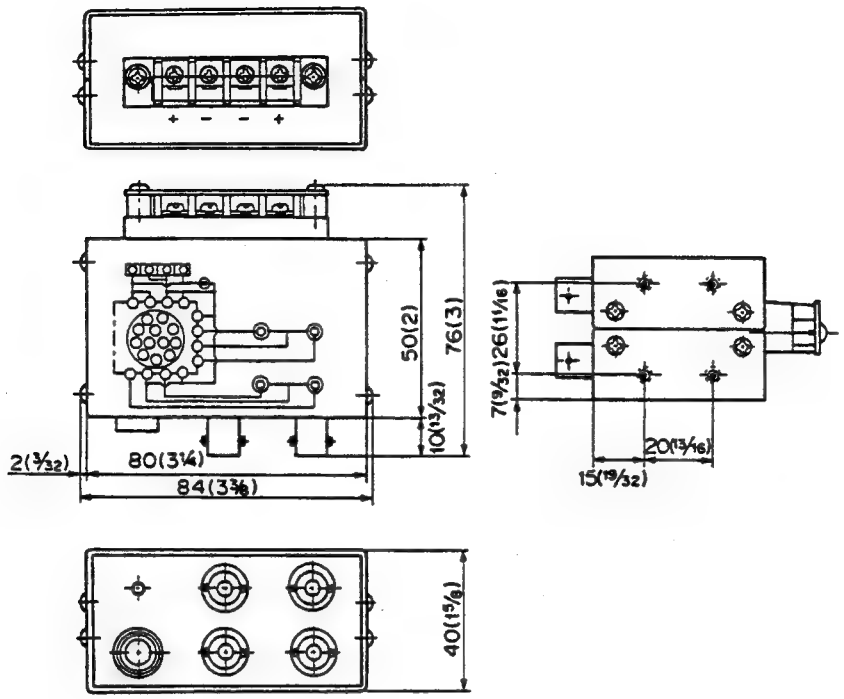




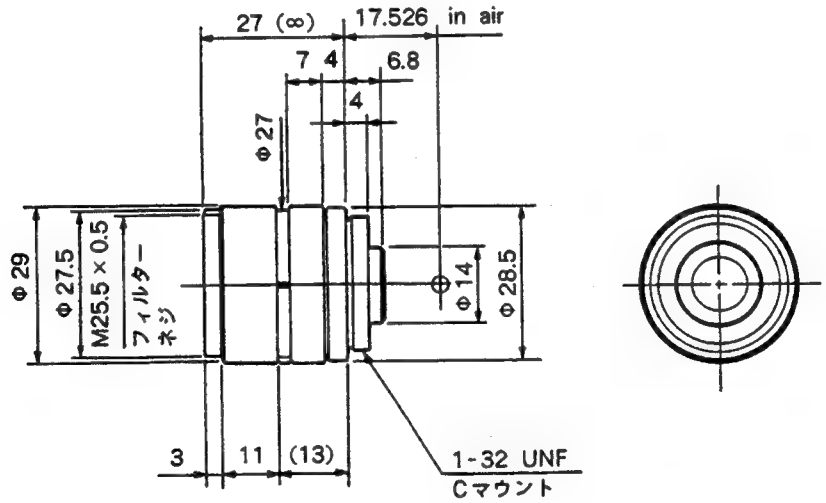



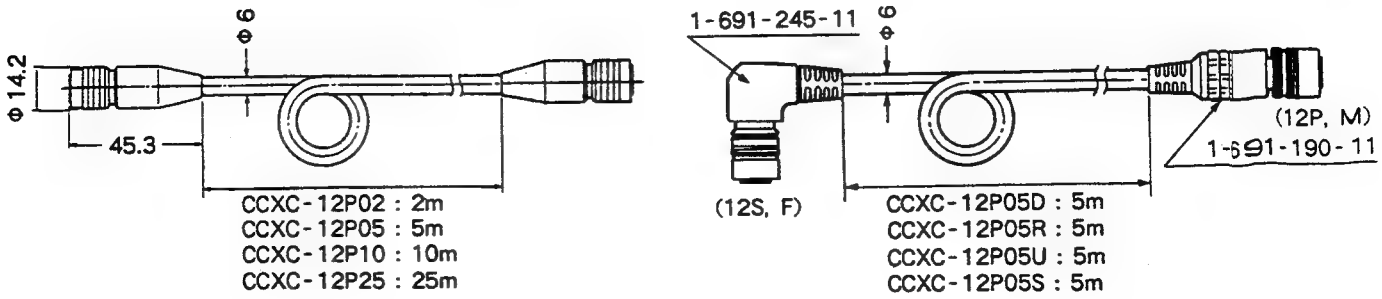
ジャンクションボックス




レンズ

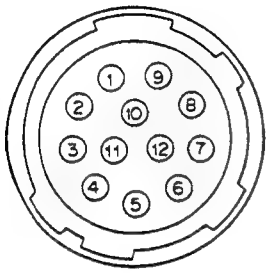



カメラケーブル



## 2-2. コネクターの入出力信号

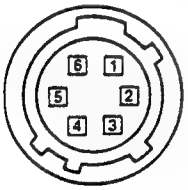
12P マルチコネクター（接続側）




| ピン番号 | 外部同期モード | | | カメラ同期信号出力 |
|---|---|---|---|---|
| | HD／VD | VS | リスタートリセット | |
| 1 | アース | アース | アース | アース |
| 2 | DC＋12V | DC＋12V | DC＋12V | DC＋12V |
| 3 | 映像出力（アース） | 映像出力（アース） | 映像出力（アース） | 映像出力（アース） |
| 4 | 映像出力（信号） | 映像出力（信号） | 映像出力（信号） | 映像出力（信号） |
| 5 | HD入力（アース） | ― | HD入力（アース） | HD出力（アース） |
| 6 | HD入力（信号） | ― | HD入力（信号） | HD出力（信号） |
| 7 | VD入力（信号） | VS入力（信号） | リセット（信号） | VD出力（信号） |
| 8 | ― | ― | ― | クロック出力（アース） |
| 9 | ― | ― | ― | クロック出力（信号） |
| 10 | アース | アース | アース | アース |
| 11 | DC＋12V | DC＋12V | DC＋12V | DC＋12V |
| 12 | VD入力（アース） | VS入力（アース） | リセット（アース） | VD出力（アース） |

（注） HD／VD入力レベルは2～5Vpp負極性
VSのSYNCレベルは0.3～1.2Vpp負極性
共に75 Ω内部終端あるいは高インピーダンス入力切り換え可能

6ピンレンズコネクター（接続側）

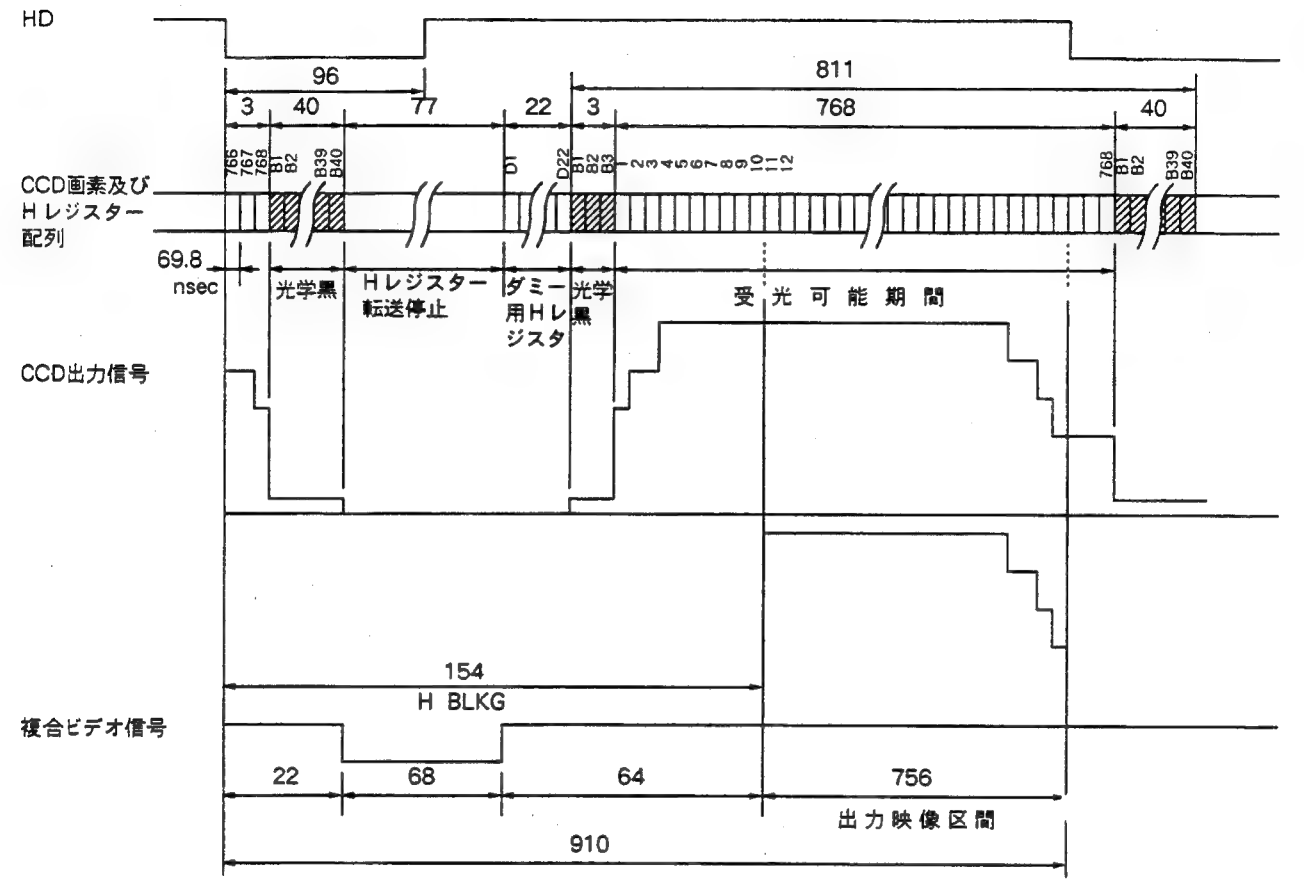


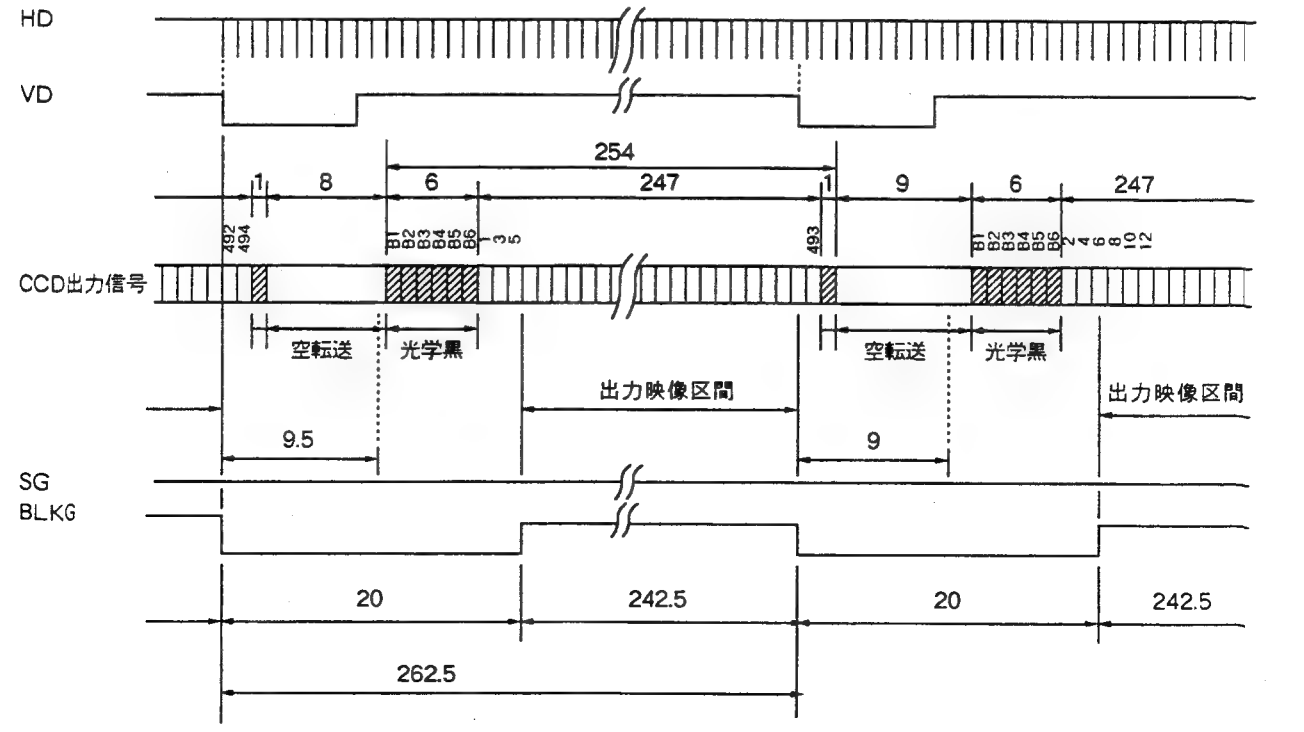

| ピン番号 | 信　号　名 | 規　　格 |
|---|---|---|
| 1 | FLD OUT | FLD信号出力 |
| 2 | トリガー | トリガー |
| 3 | GND | アース |
| 4 | NC | 空ピン |
| 5 | VS OUT | 映像信号出力　＊ |
| 6 | ＋12 OUT | DC＋12V出力 |

＊（注）
⑤Pinの映像出力は、AUTO IRISレンズ用に用意されたもので、
75 Ω終端で使用することはできません。

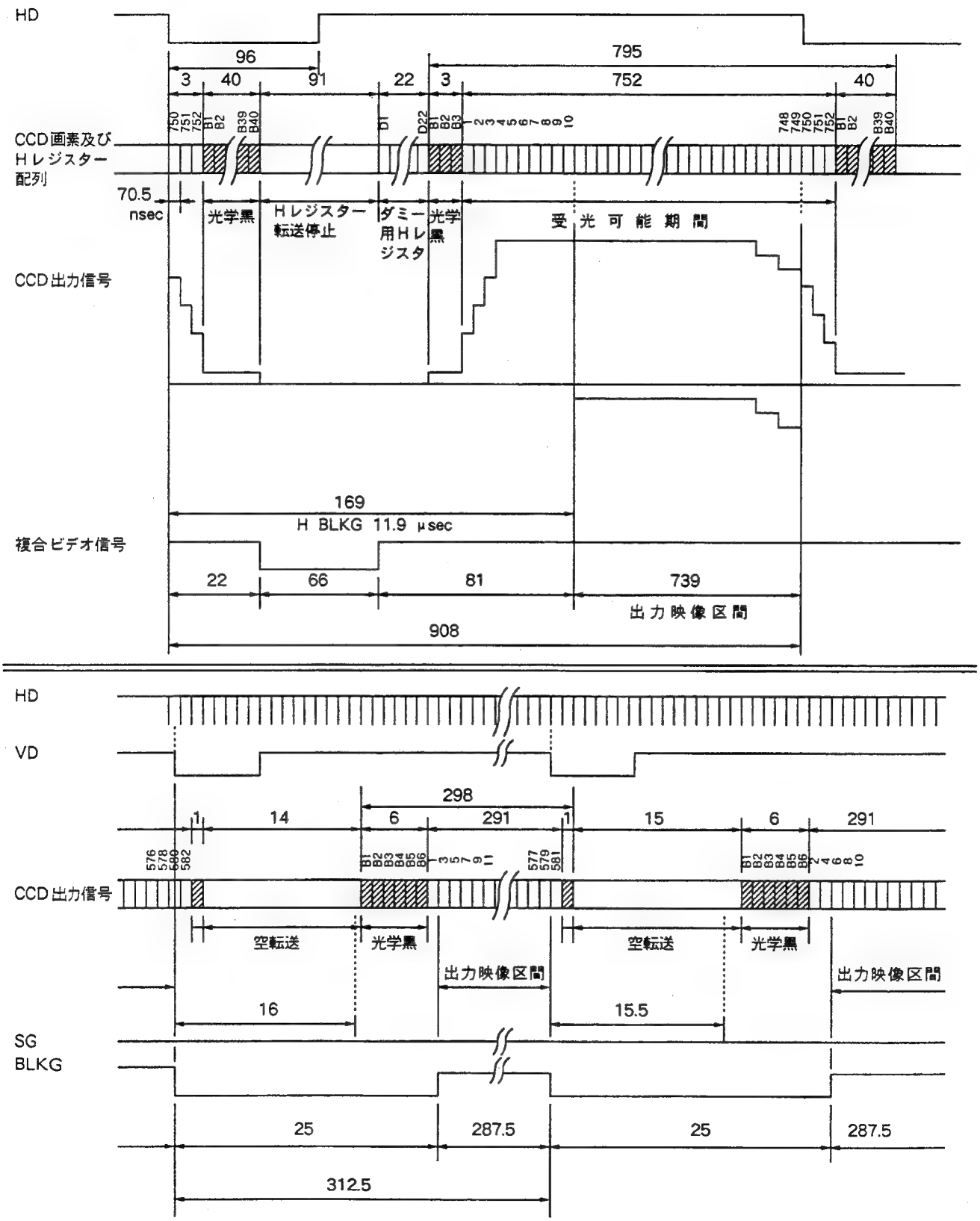
## 2-3. CCD出力波形タイミングチャート

### 2-3-1. EIA



2-3-2. CCIR


HD
96
795
3
40
91
22
3
752
40
750
751
752
B1
B2
B39
B40
D1
D22
B1
B2
B3
1
2
3
4
5
6
7
8
9
10
748
749
750
751
752
B1
B2
B39
B40
CCD画素及び
Hレジスター
配列
70.5
nsec
光学黒
Hレジスター
転送停止
ダミー
用Hレ
ジスタ
光学
黒
受光可能期間
CCD出力信号
169
H BLKG 11.9 μsec
複合ビデオ信号
22
66
81
739
出力映像区間
908
HD
VD
298
1
14
6
291
1
15
6
291
576
578
580
582
B1
B2
B3
B4
B5
B6
1
3
5
7
9
11
577
579
581
B1
B2
B3
B4
B5
B6
2
4
6
8
10
CCD出力信号
空転送
光学黒
出力映像区間
空転送
光学黒
出力映像区間
16
15.5
SG
BLKG
25
287.5
25
287.5
312.5

## 2-4. 外部同期について

外部同期モードには下記の3モードがあります。

1. VS／VBSモード
2. HD, VDモード
3. RESTART RESETモード

### 2-4-1. VS／VBSモード

正規のコンポジット信号（VSまたはVBS）を12ピンコネクターの7番ピンに加えることで外部同期を掛けるモードです。

### 2-4-2. HD, VDモード

HD, VDを12ピンコネクターの6番ピンと7番ピンにそれぞれ加えることで外部同期を掛けるモードです。

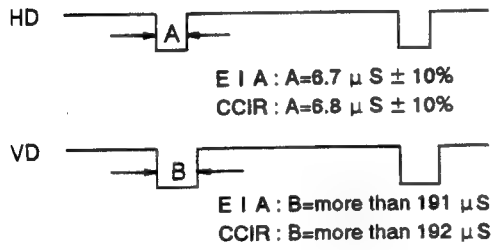
HD, VDの入力条件

●周波数（周期）

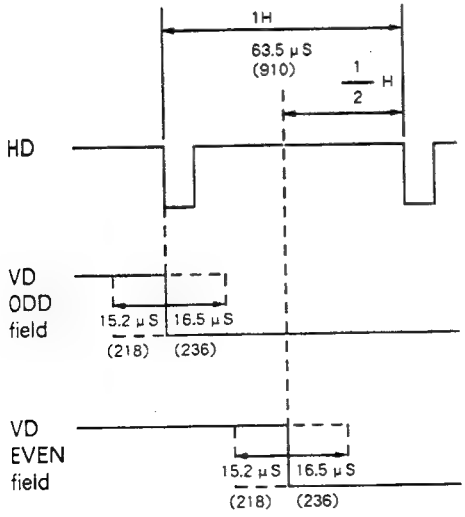
HD　15.734 kHz ± 1 %（63.56 μS ± 1 %）

VD　244～1023$\frac{1}{2}$ H

※注意：最大垂直有効ライン数はインターレース時で486ラインです。
ノンインターレース時は、ODDフィールド、EVENフィールドとも242ラインです。




●位相




＊（ ）内はクロック数

イラスト中でHDの立ち下がりに対してVDの立ち下がりが進相15.2 μS～遅相16.5 μS以内の時はODDフィールドになります。

また、HDの立ち下がりから$\frac{1}{2}$ Hの時点に対するVDの立ち下がりが進相15.2 μS～遅相16.5 μS以内の時はEVENフィールドになります。

インターレース／ノンインターレース

VDの入力条件を変化させることで、インターレースでもノンインターレースでも動作させることができます。

（〔図1〕参照）

●インターレース

インターレースで動作させる時は、VDの周期を（A + $\frac{1}{2}$）Hにします。「Aは244～1023までの整数」すなわちHDの立ち下がりに対するVDのの位相が、VD毎に切り換わります。

するとフィールドがODD→EVEN→ODD→…と変化し、インターレースで動作します。この時の1フレームの走査線数は2A + 1ラインです。

●ノンインターレース

ノンインターレースで動作させる時は、VDの周期をAHにします。「Aは244～1023までの整数」すなわちHDの立ち下がりに対するVDのの位相が、VD毎に変化せず、フィールドがODD→ODD→ODD→…、EVEN→EVEN→EVEN→…と続き、ノンインターレースで動作します。但し、1フレームの走査線数はAラインでインターレース時の半分になります。またフレーム蓄積時には感度もインターレース時の半分になります。

（〔図2〕参照）

## 2-4-3. RESTART RESETモード

RESTART RESET (R.R) モードを使うと任意の時刻に1画面の情報を取り出すことができます。
R.Rモードを使う場合は、カメラ内部でモードを設定する必要があります。
2-5. 動作モードの設定と機能を参照してモードを設定して下さい。HD, R.Rを12ピンコネクターの6番ピンと7番ピンにそれぞれ加えることで、出力を得ることができます。

HD, R.Rの入力条件

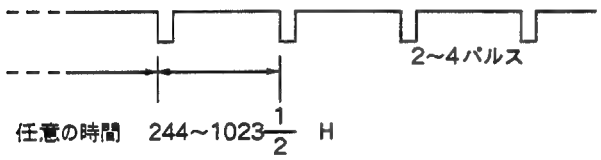
●周波数（周期）

HD 15.734 kHz ± 1 % (63.56 μS ± 1 %)

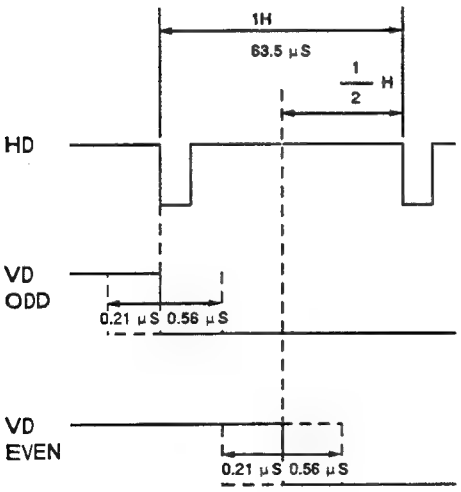
連続パルス


VD 244～1023$\frac{1}{2}$ H

2～4パルス（モードによって異なります。）




●位相




●外部入力信号 (HD, VD) の位相関係 (許容差) は、上図で示すとおり、規格中心位相に対して、＋8クロック／-3クロックの範囲です。

タイミングチャートの説明

〔図3〕は各動作モード別のタイミングチャートです。以下に詳細を説明します。

●フレーム蓄積、インターレースモード

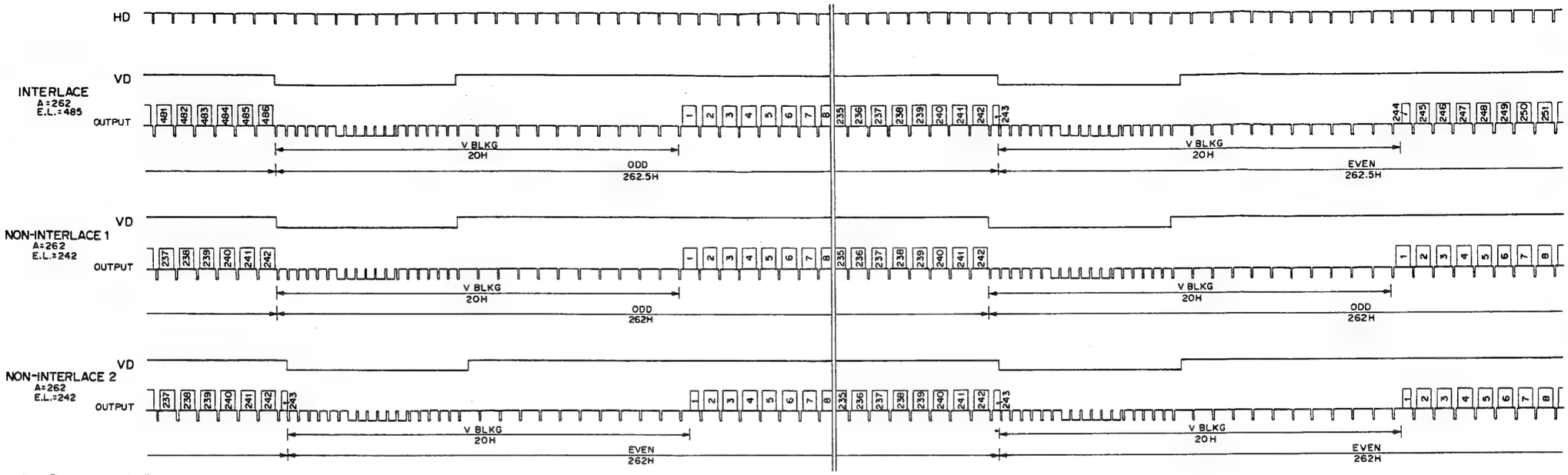
R.Rが4パルス必要です。R.Rの周期を（A + $\frac{1}{2}$）Hにします。「Aは244～1023までの整数（図はA = 262)」IMAGING C (ODD) とIMAGING D (EVEN) の期間にそれぞれSTORAGE 1, STORAGE 2の間に撮像した情報が出力されます。IMAGING A, IMAGING Bの間にCCDがリセットされます。よって、この間に出力される信号は意味がありません。

●フィールド蓄積、インターレースモード

R.Rが3パルス必要です。R.Rの周期を（A + $\frac{1}{2}$）Hにします。「Aは244～1023までの整数（図はA = 262)」IMAGING B (ODD) とIMAGING C (EVEN) の期間にそれぞれSTORAGE 1, STORAGE 2の間に撮像した情報が出力されます。IMAGING Aの期間にCCDがリセットされます。よって、この間に出力される信号は意味がありません。

●ノンインターレース

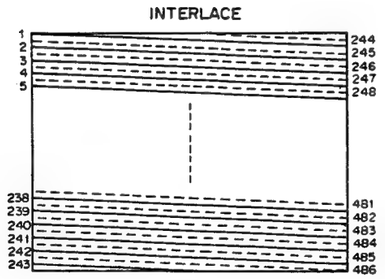
蓄積モードに関係なくR.Rが2パルス必要です。
R.Rの周期をAHにします。「Aは244～1023までの整数（図はA = 262)」
IMAGING Bの期間にSTORAGE 1の間に撮像した情報が出力されます。IMAGING Aの期間にCCDがリセットされます。よって、この間に出力される信号は意味がありません。

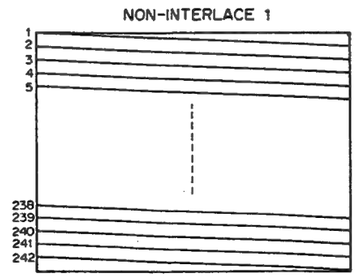


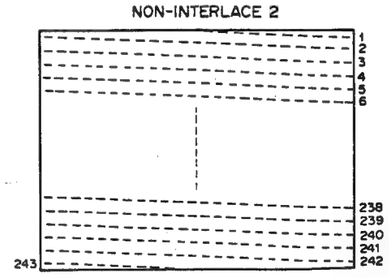

Note:EL means effective line

注意：E.L.は有効ライン数です。

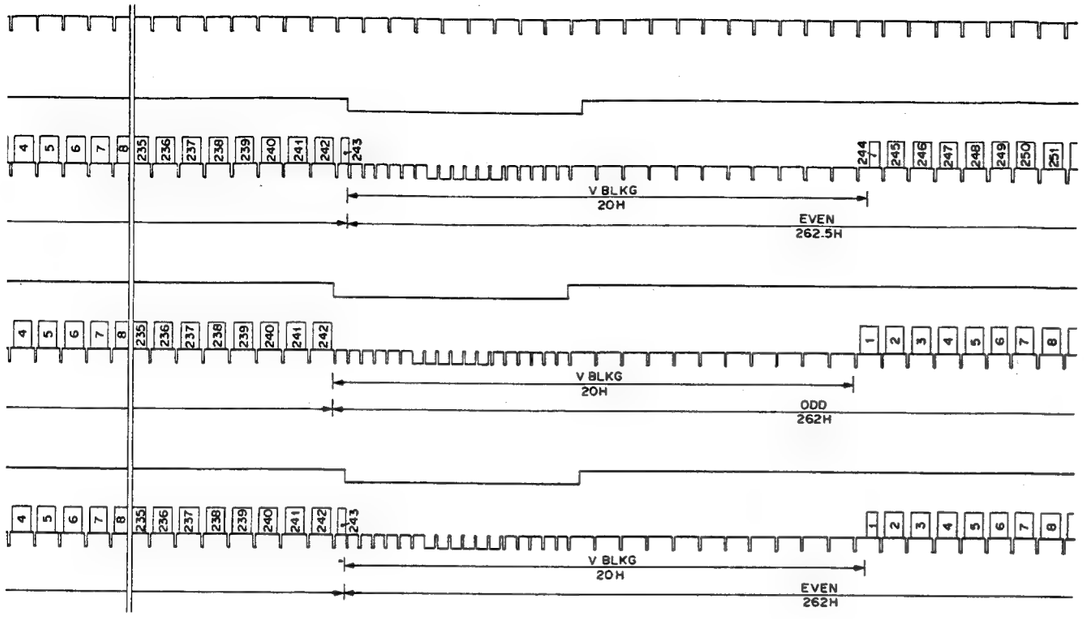
| リードアウトモード設定 | |
|---|---|
| 走査方式 | |
| 走査 | NORMAL MODE |
| | INVERSE MODE |
| 蓄積時間と映像出力の関係 | |
| 垂直解像度(TV本) | |
| RESTART RESET | |
| 特徴と用途 | |



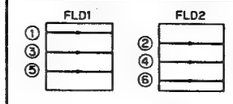
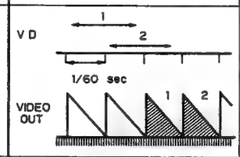
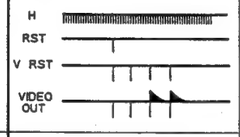



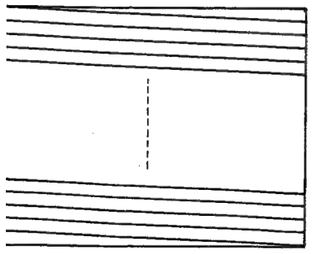

〔図1〕




〔図2〕 走査方式と蓄積モードの関係

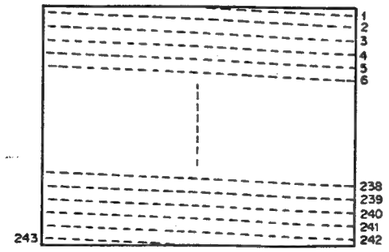
| リードアウトモード設定 | | フレーム蓄積（初期設定側） | | フィールド蓄積 | |
|---|---|---|---|---|---|
| 走査方式 | | インターレス | ノンインターレス | インターレス | ノンインターレス |
| 走査 | NORMAL MODE |  |  |  |  |
| | INVERSE MODE | FLD 1/FLD 2が逆転。 | FLD 1/FLD 2共に②，④，⑥…になる。 | FLD 1/FLD 2が逆転。 | FLD 1/FLD 2共に②，④，⑥…になる。 |
| 蓄積時間と映像出力の関係 | |  |  |  |  |
| 垂直解像度(TV本) | | 485 | 242 | 350 | 242 |
| RESTART RESET | |  |  |  |  |
| 特徴と用途 | | 最も高い解像度が得られるので，フレームメモリーを持つ計測等に適する。 | XC-39と同一システム。垂直の一本置き走査となる。注）動作はフィールド蓄積 | $\frac{1}{60}$秒の蓄積により，フレーム蓄積よりもぶれの少ない画が得られる。移動物体を補うえるのに適する。 | ノンインターレス時に，感度を落とさず，垂直の情報も全て取り入れるシステム。 |

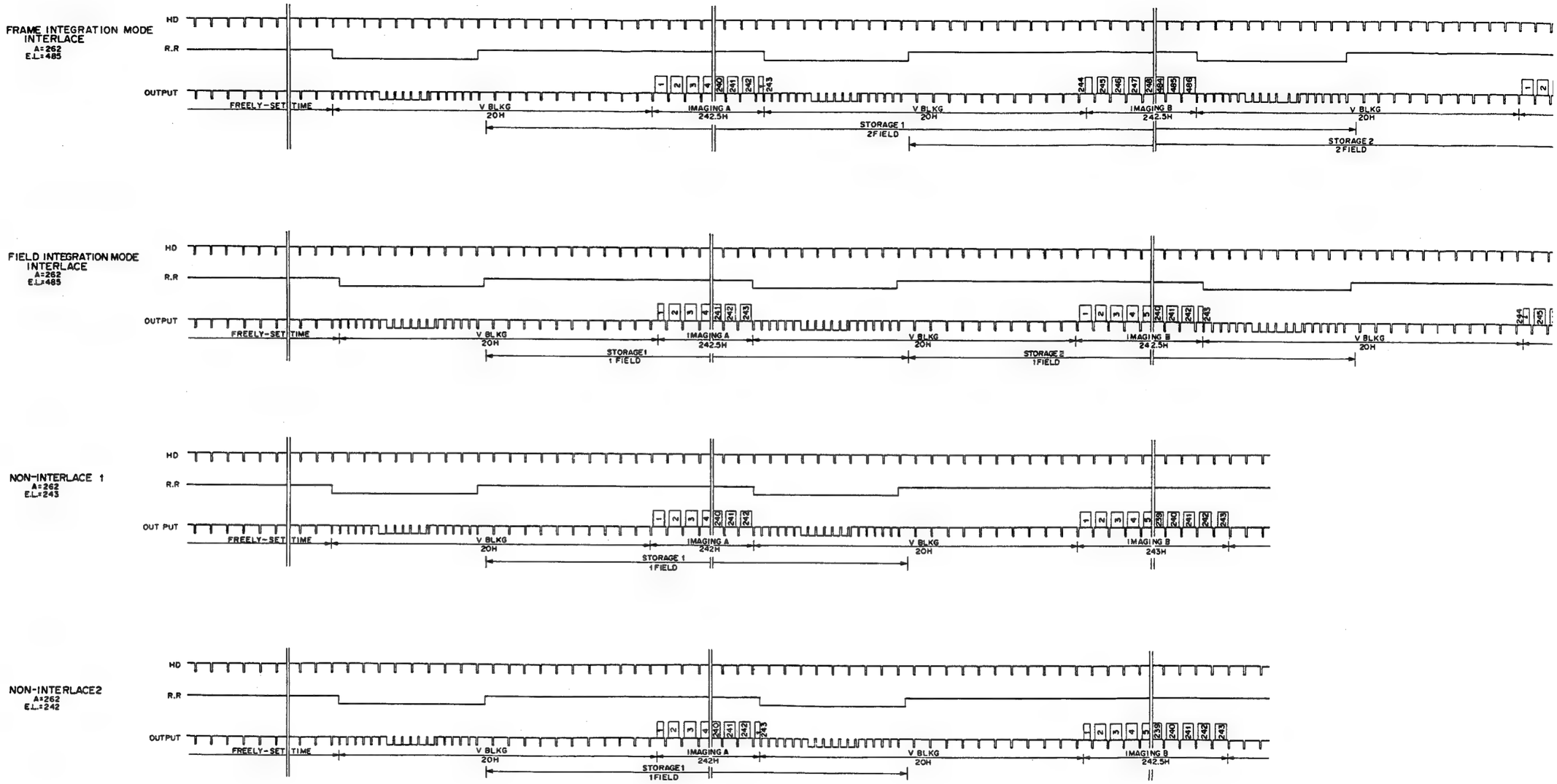
NON-INTERLACE 1



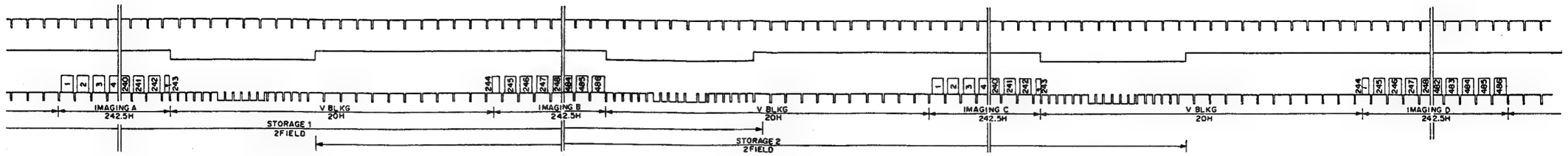
〔図1〕

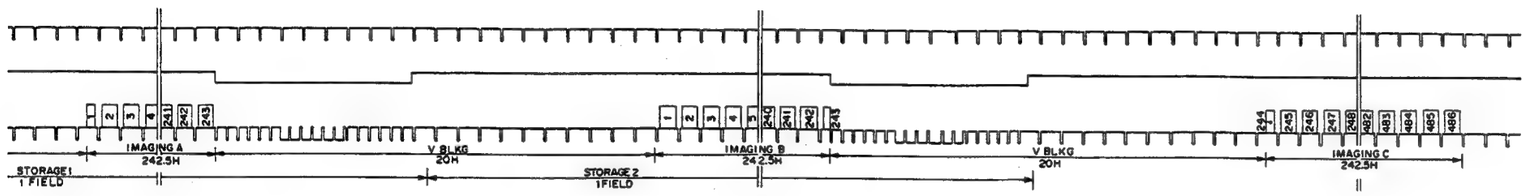
NON-INTERLACE 2

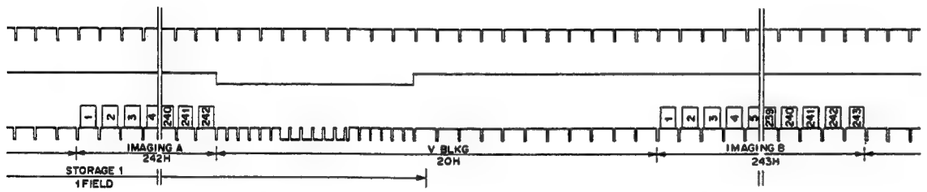


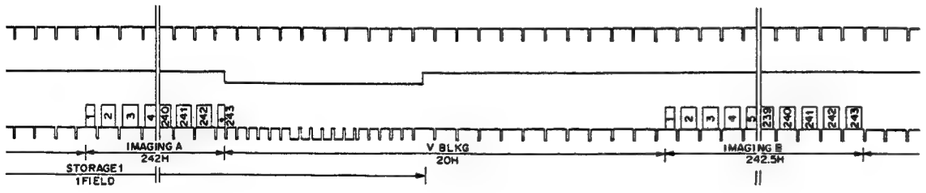

FRAME INTEGRATION MODE
INTERLACE
A=262
E.L=485
HD
R.R
OUTPUT
FREELY-SET TIME
V BLKG
20H
IMAGING A
242.5H
STORAGE 1
2FIELD
IMAGING B
242.5H
STORAGE 2
2FIELD
FIELD INTEGRATION MODE
INTERLACE
A=262
E.L=485
STORAGE1
1 FIELD
STORAGE 2
1FIELD
NON-INTERLACE 1
A=262
E.L=243
OUT PUT
IMAGING A
242H
IMAGING B
243H
NON-INTERLACE2
A=262
E.L=242
IMAGING B
242.5H

〔図3〕


IMAGING A
242.5H
V BLKG
20H
IMAGING B
242.5H
V BLKG
20H
IMAGING C
242.5H
V BLKG
20H
IMAGING D
242.5H
STORAGE 1
2FIELD
STORAGE 2
2FIELD


IMAGING A
242.5H
V BLKG
20H
IMAGING B
242.5H
V BLKG
20H
IMAGING C
242.5H
STORAGE1
1 FIELD
STORAGE 2
1FIELD


IMAGING A
242H
V BLKG
20H
IMAGING B
243H
STORAGE 1
1FIELD


IMAGING A
242H
V BLKG
20H
IMAGING B
242.5H
STORAGE1
1FIELD

〔図3〕

## 2-5. 動作モードの設定と機能

XC-73／75は、用途に応じて動作モードを切り換えることが可能です。
モード設定は、スイッチによる設定方法と半田ジャンパーによる設定方法があります。

| 番号 | 項目 | 設定場所 | 設定方法 | 工場出荷モード |
|---|---|---|---|---|
| 1 | γ補正モード | PR-165基板 | JR1, JR2※1 | OFF |
| 2 | 電子シャッターモード | MB-403基板 | ジャンパーJR1 | OPEN (NORMAL) |
| 3 | シャッターコントロールパルスの設定 | MB-403基板 | ジャンパーJR2 | OPEN |
| 4 | ノーマル電子シャッターのスピード設定 | MB-403基板 | スイッチS1 | "0" (OFF) |
| 5 | 電荷蓄積モード | MB-403基板 | ジャンパーJR3 | OPEN (FRAME) |
| 6 | 同期信号入出力 HD／VD | SG-199基板 | スイッチS1 | EXT (INPUT) |
| 7 | EXT-HD終端 ON-OFF | SG-199基板 | スイッチS2 | ON |
| 8 | EX-VD終端 ON-OFF | SG-199基板 | スイッチS3 | ON |
| 9 | H位相進相量* | SG-199基板 | ジャンパーJR1～6 | 1,2のみSHORT |
| 10 | RESTART-RESETモード* | SG-199基板 | ジャンパーJR7,8 | SHORT (OFF) |
| 11 | FIELD INVERTモード* | SG-199基板 | ジャンパーJR9 | OPEN |
| 12 | GAIN モード | リアパネル | スイッチ | FIX |
| 13 | MANUAL GAIN | リアパネル | ボリューム | 0 dB |
| 14 | CLOCK 出力モード | リアパネル | ジャンパーJR1 | OPEN |

＊：H位相進相量、RESTART-RESET、フィールド反転の設定は、外部同期モードの場合のみ有効です。
※1：PR-165基板の基板末尾が-11の場合は、JR1とJR2の代わりにスイッチS1が付いてます。
対象シリアルナンバー
XC-73 (UCJ)：10001-15550
XC-75 (UCJ)：10001-60900

1. γ補正モード（γ ON／γ OFF）

γ補正をONに設定するとγ補正の行われたVIDEO信号を出力します。

γ補正をOFFに設定するとγ補正が行われず、被写体の光量に比例したVIDEO出力信号を得ることができます。

この設定は、PR-165基板の※内部ジャンパーJR1とJR2にて行われます。

※PR-165基板の基板末尾が-11の場合は、内部ジャンパーの代わりに内部スイッチS1で行われます。

対象シリアルナンバー

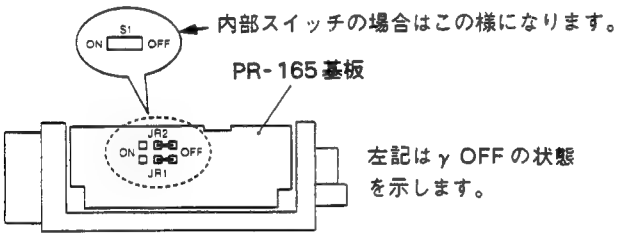
XC-73 (UCJ) : 10001-15550

XC-75 (UCJ) : 10001-60900

工場出荷時はγ OFFに設定されています。

PR-165基板

| MODE | JR1, JR2 | S1 | 入出力特性 |
|---|---|---|---|
| γ ON (0.45) | ON : 中央のランドとON側のランドをショートする。 | ON | OUT / IN |
| γ OFF (1.0) | OFF : 中央のランドとOFF側のランドをショートする。 | OFF | OUT / IN |




2. 電子シャッターモード（NORMAL／SPECIAL）

CCDによる電子シャッターのタイプを設定します。

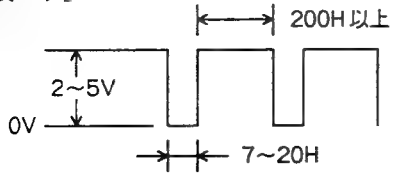
● NORMALモード

通常の電子シャッターを意味し、No.4で述べるMB-403基板のロータリースイッチ（S1）でシャッタースピードを設定します。

● SPECIALモード

ランダムタイミングの露光スタートをかけるタイプの電子シャッターで、No.3で述べるMB-403基板のジャンパーランドJR2で、露光スタートを決める入力パルスの選択を行います。

注）電源投入直後に限り、動作を開始させる為12Pコネクターの7番ピンに、下記の様な2発のリセットパルスの入力が必要です。




| モード | JR1 (MB-403) |
|---|---|
| NORMAL | OPEN |
| SPECIAL | SHORT |

3. シャッターコントロールパルスの設定

SPECIALモードの電子シャッターの露光スタートを決めるVDおよびTR入力パルスの選択が可能です。

● VDを選択した場合

内部VDパルスの立ち下がりタイミングが露光スタート直前の最終シャッターパルスの位相となるため、この位相から約2.0 μsec後の露光スタートとなります。

シャッタースピードは、CCDのタイプ／フィールドで、それぞれ一義的に設定されます。

● TRを選択した場合

リアパネルの6Pコネクター（2番ピン）から入力されるパルスの立ち上がりタイミングが露光スタート直前の最終シャッターパルスの位相となるため、この位相から約2.0 μsec後の露光スタートとなります。

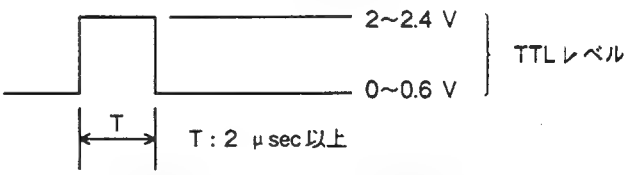
シャッタースピードは、上記入力パルスと外部同期用VDの位相差で決まり、任意に設定できます。

●外部から電子シャッターのシャッタースピードをコントロールする場合

SPECIALモードに設定し、入力パルスをTRに設定します。この状態で、SG-199基板のS1スイッチをI（またはINT）に設定して、内部HD／VD出力パルスをカメラから取り出します。このパルスをもとにしてコントロールパルスを作成します。作成されたコントロールパルスをリアパネルの6ピンコネクター（2番ピン）に入力することにより、外部からのからのシャッタースピード設定が可能となります。

〔シャッターコントロールパルスの規定〕

リアパネル6Pコネクター（2番ピン）入力

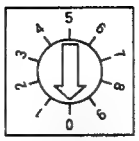



4. ノーマル電子シャッターのスピード設定

NORMALモードの電子シャッターのスピードを設定します。

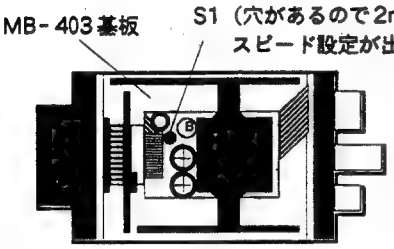
シャッタースピードおよびフリッカーレスモードの設定はMB-403基板のロータリーコードスイッチ（S1）で行います。

| 位置 | シャッタースピード |
|---|---|
| 0 | OFF |
| 1 | 1／125 |
| 2 | 1／250 |
| 3 | 1／500 |
| 4 | 1／1000 |
| 5 | 1／2000 |
| 6 | 1／4000 |
| 7 | 1／10000 |
| 8 | フリッカーレスモード* |
| 9 | フリッカーレスモード* |



MB-403基板
スイッチ（S1）
（工場出荷時設定）

＊：フリッカーレスモードはポジション8，9で設定できます。
8，9どちらにおいてもEIAでは1／100 sec. CCIRでは
1／120 sec.に設定されます。




＊モニタを見てシャッターOFFを確認する方法
条件：レンズの“F値”を固定する。
a，b、どちらかの方法で確認する事ができます。

a）MB-403基板の“S1”を時計方向に回していき、映像が最も明るい位置がシャッターOFFの位置になります。

b）MB-403基板の“S1”を時計方向に回していくと、映像の明るさ変動の無い位置が続けて2ヶ所あります。その位置からさらに1つ先に回すとそこがシャッターOFFの位置になります。

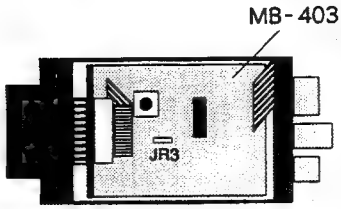
5. 電荷蓄積モード

CCDのフォトセンサーから信号電荷を読み出す周期を設定します。

- FIELDに設定すると信号出荷を2群の画素から同時に読み出すフィールド蓄積モードになります。
- FRAMEに設定すると、信号電荷を2群の画素から交互に読み出すフレーム蓄積モードになります。
- フレーム蓄積モードは、インターレース動作時に比べてノンインターレース動作では、感度が半分になります。（2-11頁の〔図2〕を参照）

設定は、MB-403基板のジャンパーランドJR3で行います。JR3をショートするとFIELDになります。またオープンするとFRAMEになります。

工場出荷時は、FRAMEに設定されています。



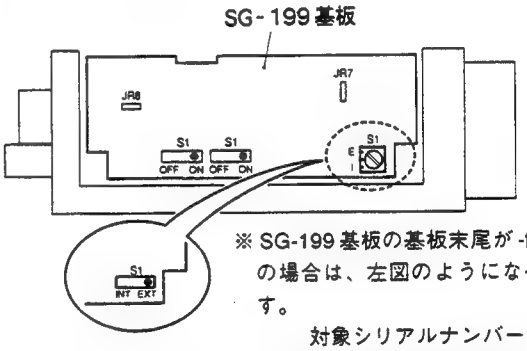

6. 同期信号入出力HD／VD

同期信号を外部出力するか、外部入力するかを設定します。
設定は、SG-199基板のスイッチS1で行います。
外部同期モードにする場合は、表示「＊E」側に、内部同期モードにする場合は表示「＊I」側にS1を設定します。

※SG-199基板の基板末尾が-11と-12の場合は、「EXT」および「INT」で表示されています。
対象シリアルナンバー
XC-73 (UCJ)：10001-15750
XC-75 (UCJ)：10001-63900

- EXTERNAL（外部同期モード）に設定すると、外部入力した同期信号（HD，VD信号など）に同期させたVIDEO出力信号が得られます。
- INTERNAL（内部同期モード）に設定すると内部で発生している同期信号を外部出力することができます。

工場出荷時は、外部同期モード（EXTERNAL）に設定されています。




※SG-199基板の基板末尾が-11と-12の場合は、左図のようになっています。
対象シリアルナンバー
XC-73 (UCJ)：10001-15750
XC-75 (UCJ)：10001-63900

外部同期入力インピーダンス変更方法

| ＊ハイインピーダンス入力にする時は | | |
|---|---|---|
| SG-199基板 | | |
| S2 | OFF | HD信号 |
| S3 | OFF | VD信号 |

内部同期信号“HD”，“VD”を出力する方法

| SG-199基板 | | |
|---|---|---|
| S1 | INT | |
| S2 | OFF | HD信号 |
| S3 | OFF | VD信号 |

7. EXT-HD終端 ON-OFF

外部からのHD入力信号を75 Ωで終端します。

設定は、SG-199基板のスイッチS2で行います。75 Ωで終端したい場合は、表示「ON」側に、終端しないときは表示「OFF」側にS2を設定します。

注意：「OFF」を選択した場合は、100 kΩ以上のハイインピーダンス受けとなります。

HD出力信号を得るためには、「OFF」側にS2を設定します。

8. EXT-VD終端 ON-OFF

外部からのVD入力信号を75 Ωで終端します。

設定は、SG-199基板のスイッチS3で行います。75Ωで終端したい場合は、表示「ON」側に、終端しない場合は表示「OFF」側にS3を設定します。

注意：「OFF」を選択した場合は、100 kΩ以上のハイインピーダンス受けとなります。

VD出力信号を得るためには、「OFF」側にS3を設定します。

9. H位相進相量

HD／VDによる外部同期時、外部入力したHD位相に対して、内部で発生するHD位相を進相させることができます。進相量の設定は、SG-199基板のジャンパーランドJR1～6で行います。

| ジャンパーランド | H進相量 |
|---|---|
| JR1 | 1 bit |
| 2 | 2 |
| 3 | 4 |
| 4 | 8 |
| 5 | 16 |
| 6 | 32 |

1 bit ≒ 70 ns

(例) 1 μs進相させたいとき

1000 ns ÷ 70 = 14.3

この場合の設定は下記のとおりです。

- JR2, 3, 4をショートする

  2 + 4 + 8 = 14 bit × 70 = 980 ns = 0.98 μs

- JR1, 2, 3, 4をショートする

  1 + 2 + 4 + 8 = 15 bit × 70 = 1050 ns = 1.05 μs

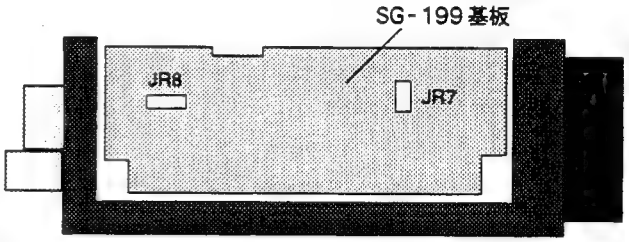
なお、工場出荷時は、JR1, 2がショート状態に設定されています。

10. RESTART RESETモード (R.Rモード)

外部同期モードにおいて、任意の時刻に1画面の情報を取り出すモードです。

設定は、SG-199基板のJR7, 8で行います。

| ジャンパーランド | NORMAL | R.R |
|---|---|---|
| JR7 | SHORT | OPEN |
| JR8 | SHORT | OPEN |



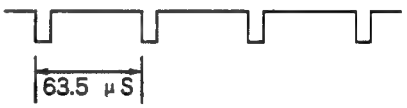

R.Rモードを選択した場合は外部同期入力信号が必要となります。HD、R.Rを12ピンコネクターの6番ピン（HD信号）と7番ピン（R.R）にそれぞれ加える事で、出力を得る事が出来ます。

条件：HD／R.Rレベル 2～5 Vp-p

周波数（周期）

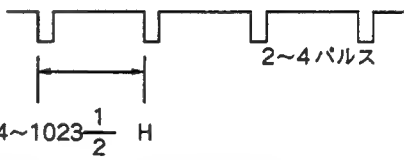
HD 15.734 kHz ± 1 %（63.56 μS ± 1 %）

連続パルス




VD 244～1023$\frac{1}{2}$ H

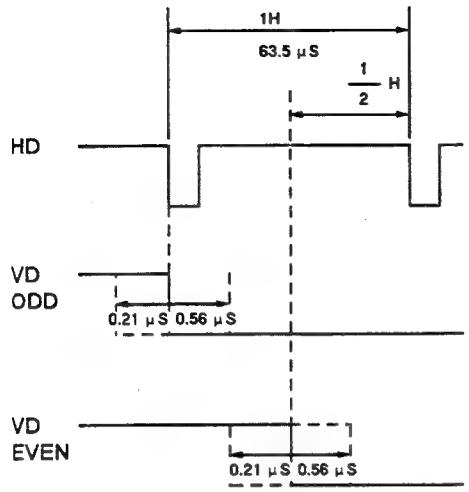
2～4パルス（モードによって異なります。）




任意の時間 244～1023$\frac{1}{2}$ H

- HDは連続したHD信号を入力する必要があります。
- VDの位相はHDに対して下記の範囲（+8クロック／-3クロック）で入力してください。

位相




●外部入力信号（HD, VD）の位相関係（許容差）は、上図で示すとおり、規格中心位相に対して、＋8クロック／−3クロックの範囲です。
工場出荷時は、NORMALに設定されています。

| フレーム蓄積 | | フィールド蓄積 | |
|---|---|---|---|
| インターレス | ノンインターレス | インターレス | ノンインターレス |
| R.Rパルス | | | |
| 4 | 2 | 3 | 2 |

11. FIELD INVERTモード
外部同期入力時にVIDEO出力信号のフィールド反転動作を設定します。
設定は、SG-199基板のジャンパーランドJR9で行います。
JR9をショートするとINVERSEモード、オープンでNORMALモードに設定されます。
- INVERSEに設定すると、VIDEO出力信号のフィールドが外部同期信号に対して反転します。外部同期信号のフィールドがODDのときはEVEN、EVENのときはODDを出力します。
- NORMALに設定すると、通常の外部同期時と同じで外部周期信号のフィールドがODDのときはODD、EVENのときはEVENを出力します。

工場出荷時は、オープンでNORMALモードに設定されています。

12. GAINモード（AUTO／FIX／MANUAL）
VIDEO出力信号のゲイン（利得）を設定します。
AUTOモードに設定すると、AGC（Automatic Gain Control）機能が働きます。AGCの最大ゲインは＋18 dBです。
FIXモードでは、ゲインが0 dBに固定されます。
MANUALモードでは、リアパネルのボリュームで、ゲインを0〜＋18 dBの範囲でGAINを可変することができます。

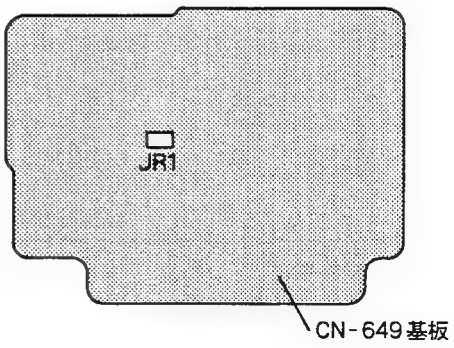
| 表示 | モード |
|---|---|
| A | AUTO GAIN |
| F | FIX GAIN |
| M | MANUAL GAIN |

工場出荷時は、FIX GAINに設定されています。

13. MANUAL GAINコントロール
GAINモードのスイッチをMANUAL GAINに設定すると、VIDEO出力信号のGAINが可変できます。
Min : 0 dB
Max : + 18 dB
工場出荷時は、0 dBに設定されています。

14. CLOCK出力モード
CLOCK出力を得たい場合、CN-649のJR1をショートすることにより12Pカメラコネクターの9番ピンからクロックが出力されます。

| 出力レベル | 5Vp-p |
|---|---|
| 出力インピーダンス | 75 Ω |



SPECIALモード設定（1）

| | 固定 | 任意 |
|---|---|---|
| Timing | ○ | − |
| Speed | ○ | − |

●SPECIALモード設定 (1) にするためには、表にしたがって確認、または変更を行ってください。
(SPECIALモード設定のために必要なジャンパーの基板配置図は2-25(J)ページに記載してあります。)

● MB-403基板

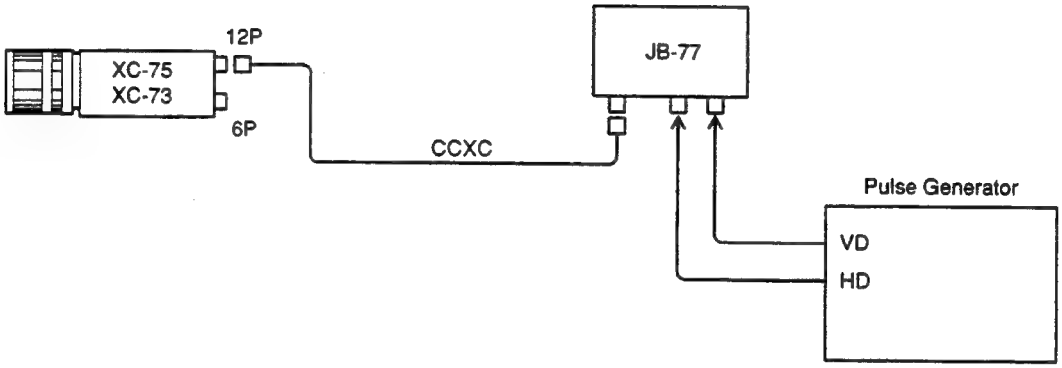
| | |
|---|---|
| JR1 | SHORT |
| JR2 | SHORT(VD) |
| JR3※ | SHORT |

● SG-199基板

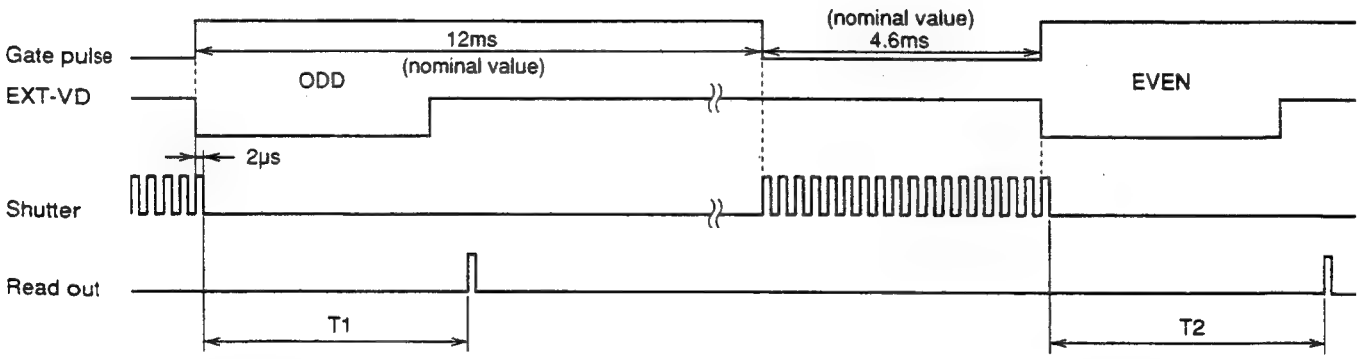
| | |
|---|---|
| S1 | EXT |
| JR7 | SHORT |
| JR8 | SHORT |

※ SHORTすることにより、FIELDモードになります。
OPENにすると、FRAMEモードになりますが、感度が1／2になります。

●接続




●パルスタイミング




| STANDARD | FIELD | EXPOSURE TIME | SHUTTER SPEED |
|---|---|---|---|
| EIA | T1 | 9H + 42.2 μs | 1／1630 s |
| | T2 | 8.5H + 42.2 μs | 1／1720 s |
| CCIR | T1 | 14.5H + 43.3 μs | 1／1030 s |
| | T2 | 14H + 43.3 μs | 1／1070 s |

SPECIALモード設定 (2)

| | 固定 | 任意 |
|---|---|---|
| Timing | − | ○ |
| Speed | ○ | − |

●SPECIALモード設定 (2) にするためには、表にしたがって確認、または変更を行ってください。
この設定により、NORMALモードからR.Rモードになります。
(SPECIALモード設定のために必要なジャンパーの基板配置図は2-25(J)ページに記載してあります。)

● MB-403基板

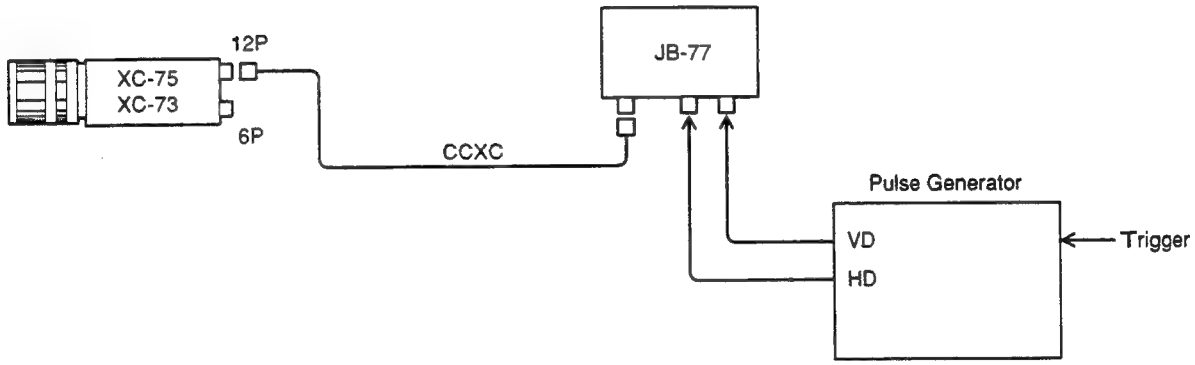
| | |
|---|---|
| JR1 | SHORT |
| JR2 | SHORT(VD) |
| JR3※ | SHORT |

● SG-199基板

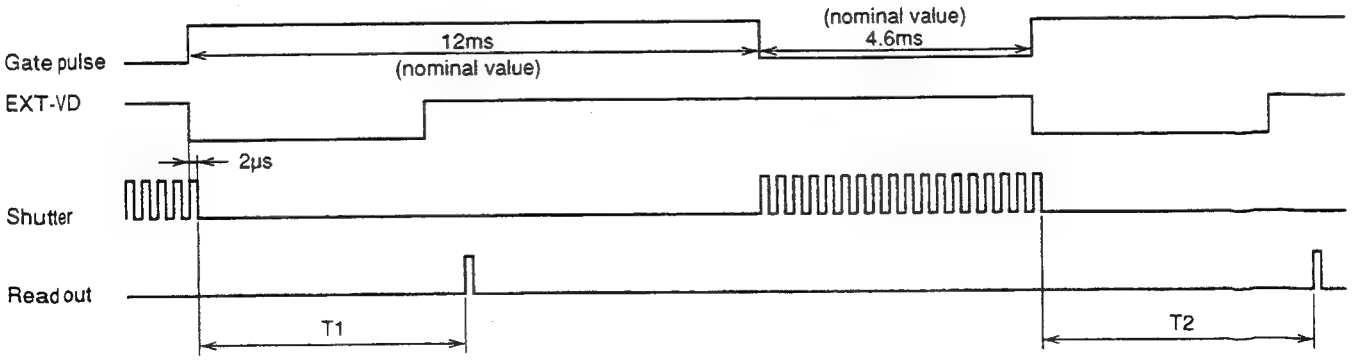
| | |
|---|---|
| S1 | EXT |
| JR7 | OPEN |
| JR8 | OPEN |

※ SHORTすることにより、FIELDモードになります。
OPENにすると、FRAMEモードになりますが、感度が1／2になります。

●接続




●パルスタイミング




● T1についてはSPECIALモード設定 (1) を参照して下さい。
● R.Rモードのため、VDはHDによるラッチが必要です。

SPECIALモード設定 (3)

| | 固定 | 任意 |
|---|---|---|
| Timing | – | ○ |
| Speed | – | ○ |

● SPECIALモード設定 (3) にするためには、表にしたがって確認、または変更を行ってください。
この設定により、NORMALモードからR.Rモードになります。
(SPECIALモード設定のために必要なジャンパーの基板配置図は2-25(J)ページに記載してあります。)

● MB-403基板

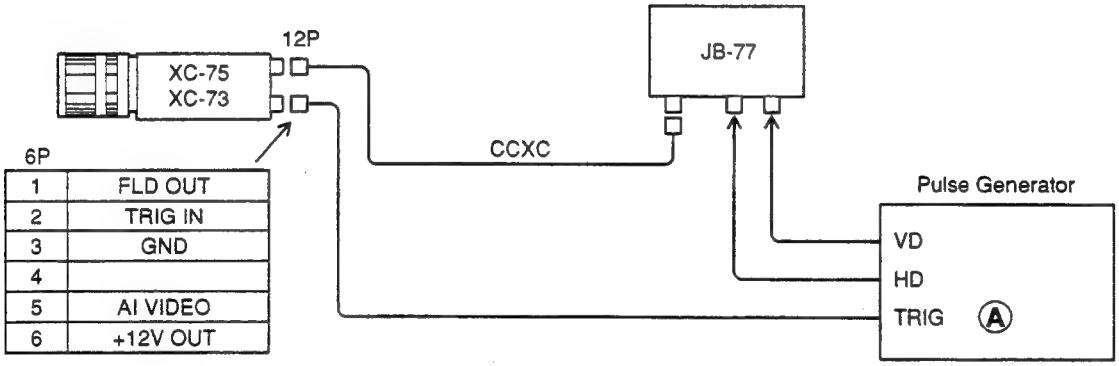
| | |
|---|---|
| JR1 | SHORT |
| JR2 | SHORT(TR) |
| JR3※ | SHORT |

● SG-199基板

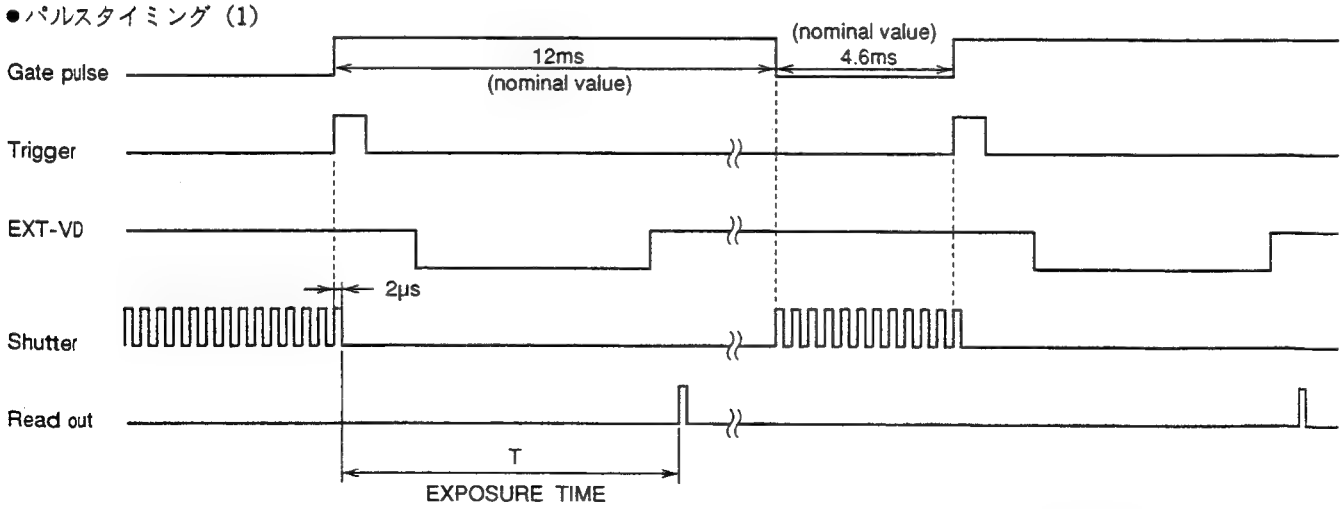
| | |
|---|---|
| S1 | EXT |
| JR7 | OPEN |
| JR8 | OPEN |

※ SHORTすることにより、FIELDモードになります。
OPENにすると、FRAMEモードになりますが、感度が1／2になります。

●接続

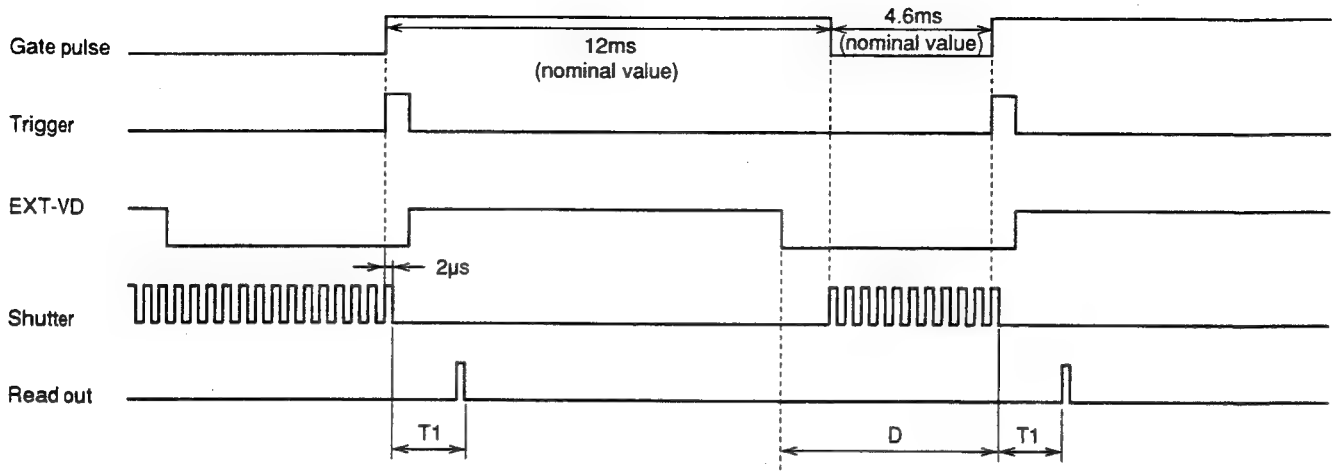



●パルスタイミング (1)



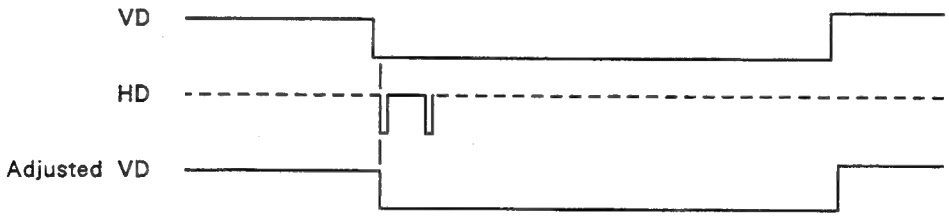

| STANDARD | FIELD | EXPOSURE TIME | SHUTTER SPEED |
|---|---|---|---|
| EIA | ODD | MAX 13 ms | 1／77 s |
| CCIR | EVEN | MAX 13 ms | 1／77 s |

●パルスタイミング (2)




| STANDARD | FIELD | EXPOSURE TIME | SHUTTER SPEED |
|---|---|---|---|
| EIA | ODD | MIN 2 μs | 1/500000 s |
| CCIR | EVEN | MIN 2 μs | 1/500000 s |

注意 1. R.Rモードのため、VDはHD位相に合わせます。




2. 任意のトリガーによるシャッターの場合、通常VDはトリガーパルス後に発生させるため最高速シャッタースピードは下記のとおりです。
   EIA : 1/1548 s
   CCIR : 1/997 s
3. VDに対してトリガー発生を遅らせた場合、超高速シャッターが得られます。

| STANDARD | FIELD | EXPOSURE TIME | SHUTTER SPEED |
|---|---|---|---|
| EIA | T1 | (9H + 42.2 μS) -D | MIN 1/500000 s |
| CCIR | T1 | (14.5H + 43.3 μS) -D | MIN 1/500000 s |

D : VDに対するトリガーパルスの遅れ

SPECIALモード設定 (4)

(SHUTTER SPEED 外部コントロールへの応用)

SPECIALモード設定 (4) にするためには、表にしたがって確認、または変更を行ってください。
(SPECIALモード設定のために必要なジャンパーの基板配置図は2-25(J)ページに記載してあります。)

● MB-403基板

| | |
|---|---|
| JR1 | SHORT |
| JR2 | SHORT(TR) |
| JR3※ | SHORT |

● SG-199基板

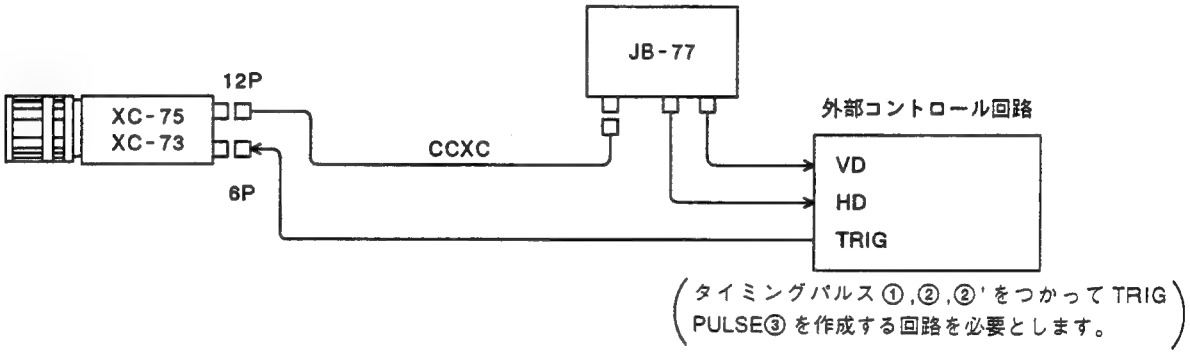
| | |
|---|---|
| S1 | INT |
| JR7 | SHORT |
| JR8 | SHORT |

● SG-199基板

| | |
|---|---|
| S2 | OFF |
| S3 | OFF |

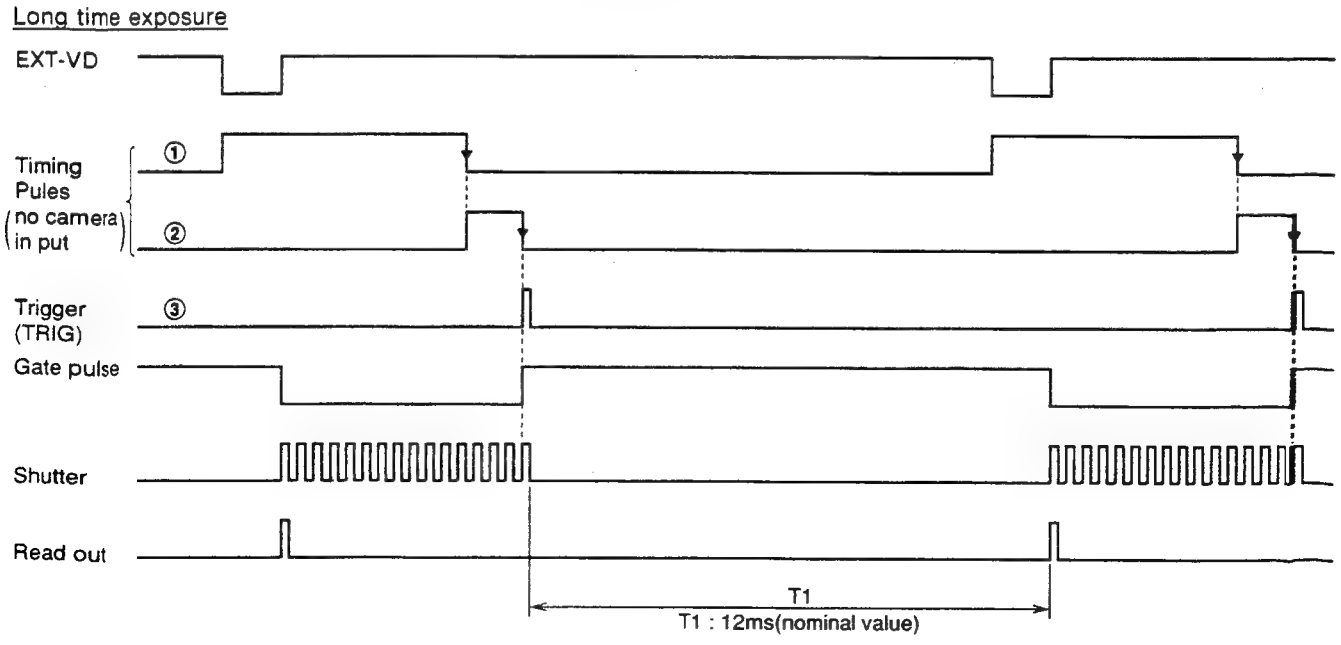
※ SHORTすることにより、FIELDモードになります。
OPENにすると、FRAMEモードになりますが、感度が1／2になります。

●接続

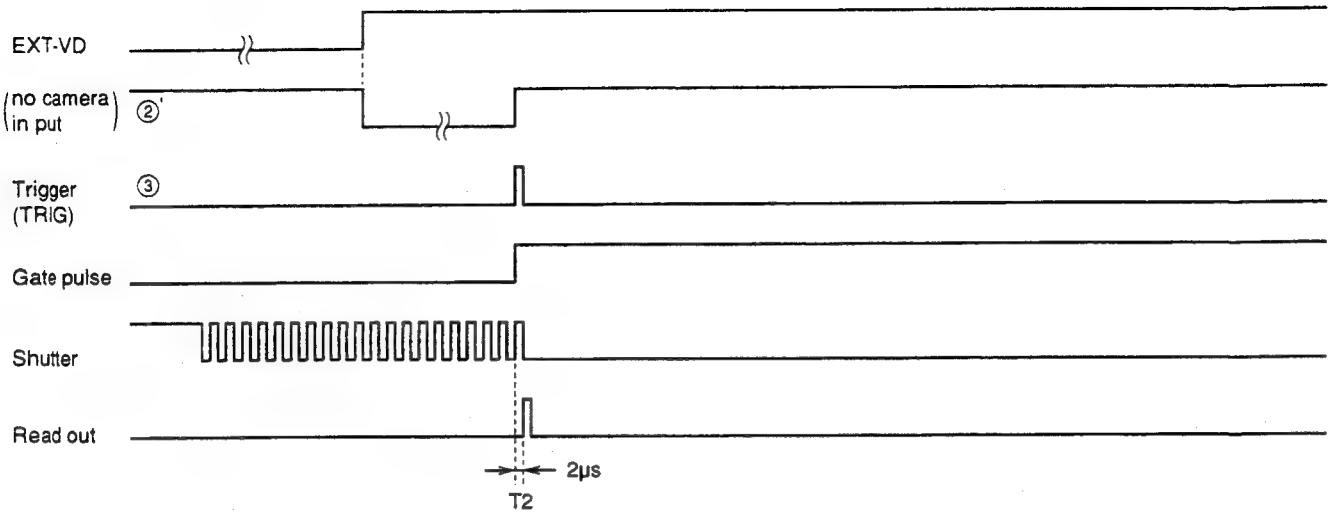



(タイミングパルス①,②,②'をつかってTRIG PULSE③を作成する回路を必要とします。)

●パルスタイミング (EXPOSURE TIME : T1～T2の連続可変が可能)

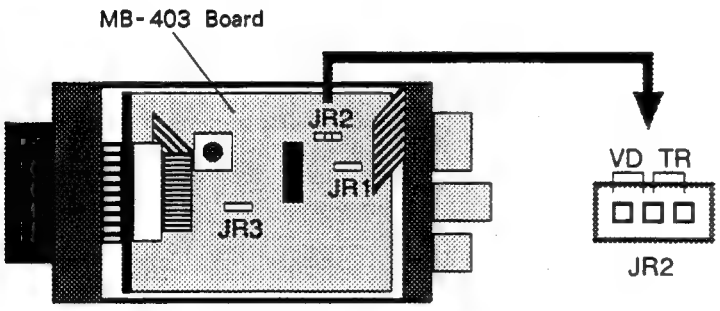


Short time exposure

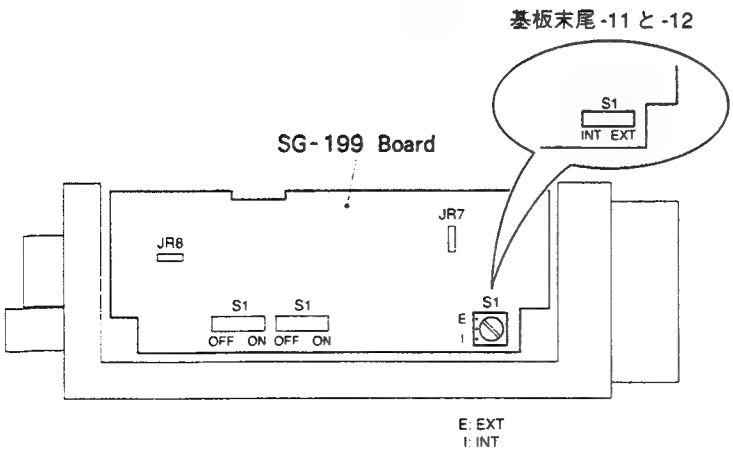



SPECIALモード設定のための基板配置図

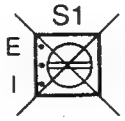
● MB-403基板




● SG-199基板




注意；
S1を中間の位置に設定すると正しい動作をしませんので中間位置に設定しないで下さい。



## 2-6. 動作説明

### 2-6-1. CCDの動作原理

CCD (Charge Coupled Device＝電荷結合ディバイス) は、規制正しく配列されたMOS (Metal-Oxide-Semiconductor) キャパシターによって構成されています。
MOSキャパシターは電荷を扱うための3つの基本的な機能を持っています。

1. 光電変換 (フォトセンサー)
   入射光は、MOSキャパシターで電荷を発生させます。このとき発生する電荷量は、光の明暗に比例します。
2. 電荷蓄積
   MOSキャパシターの電極に電圧がかけられると、シリコンの層の中の電位の井戸が作られます。電荷はこの井戸に蓄えられます。
3. 電荷の転送
   高い電圧が電極にかけられるとより深い井戸が作られ、また低い電圧では、浅い井戸が作られます。
   電荷の転送は、この特性を利用して行われます。電極に高い電圧を加えると、深い電位の井戸ができて、隣の井戸にたまっていた電荷が流れこんできます。これが規則的に並んだ電極に次々繰り返されると、電荷は1つのMOSキャパシターより次のMOSキャパシターへと移っていきます。これがCCD電荷転送の原理です。

### 2-6-2. CCDの電荷転送の機構

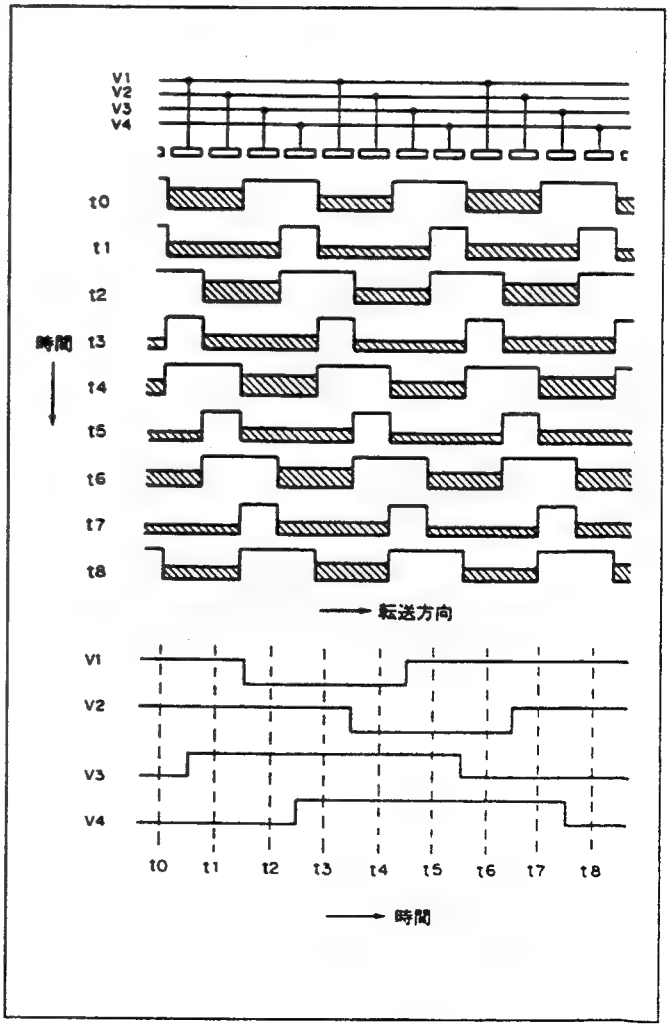
XC-75, XC-73が採用しているインターライン転送方式は、CCD上に結んだ像の明暗に対応した電荷を、2-27頁の〔図3〕のように順次転送して行くものです。フォトセンサー (感光素子) で検知した被写体の明暗に対応した電荷は、まず、それぞれ隣りの垂直転送部に転送され、垂直転送部に移った電荷は、垂直方向に順次、水平転送部へ送られます。水平転送部に移された電荷は、水平方向に順次転送され、出力部から出力されます。

#### 1. 垂直転送

垂直転送部は、4相駆動で電荷を転送しています。〔図1〕に、各時刻での電位の井戸の様子を示します。
t0の時間の状態をみると、電極電圧は (V1＝V2) ＞ (V3＝V4) となっていますので、電圧が高いV1とV2の電極の部分は井戸が深くなり、この深い部分に電荷が蓄えられています。
時刻t1では、電極電圧が (V1＝V2＝V3) ＞ (V4) となり、V1とV2とV3の井戸に電荷が蓄えられます。
時刻t2では、電極電圧が (V2＝V3) ＞ (V4＝V1) となり、V2とV3の井戸に電荷が蓄えられます。
時刻t3以降の電極電圧の状態を次に示します。

時刻t3 (V2＝V3＝V4) ＞ (V1)
時刻t4 (V3＝V4) ＞ (V1＝V2)
時刻t5 (V4) ＞ (V1＝V2＝V3)
時刻t6 (V4＝V1) ＞ (V2＝V3)
時刻t7 (V4＝V1＝V2) ＞ (V3)
時刻t8 (V1＝V2) ＞ (V3＝V4)〔時刻t0の状態と同じ〕

この動作を次々に繰り返して垂直転送が行われます。




〔図1〕垂直転送

2. 水平転送

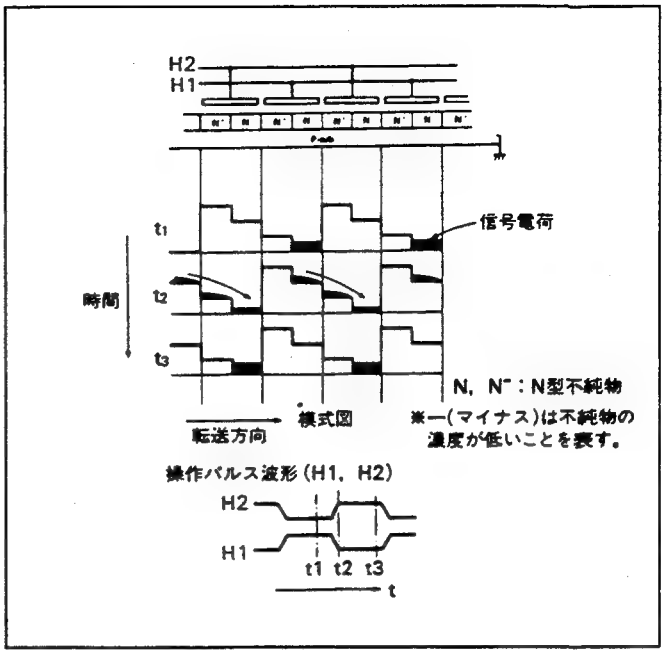
水平転送部は、2相駆動で電荷を転送しています。〔図2〕に各時間での電位の井戸の様子を示します。

時刻t1の状態をみると、電極電圧はH1＞H2となっていますので、電圧が高いH1の電極の部分は井戸が深くなり、この深い井戸の部分に電荷が蓄えられています。

時刻t2の状態では、H1, H2の電圧が反転しており、H2の井戸は深く、H1の井戸は浅くなり、H2の井戸がH1の井戸よりも深くなるので信号電荷は、深いH2の井戸の方へ流れ込みます。

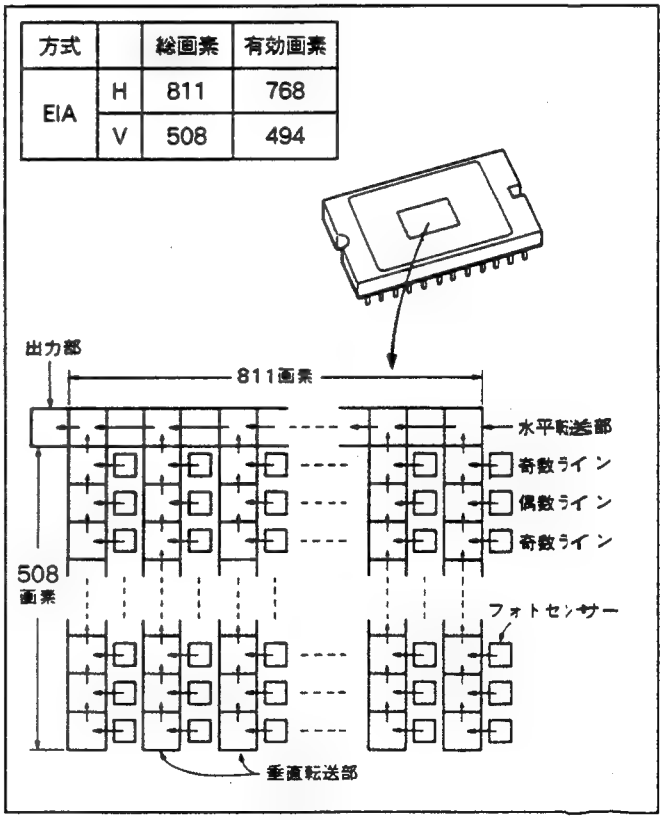
時刻t3の状態では、電極電圧は変化していないから、信号電荷は、H2の井戸へ流れ込み1つの電荷転送が完了します。

この動作を次々に繰り返して水平転送が行われます。




〔図2〕水平転送

| 方式 | | 総画素 | 有効画素 |
|---|---|---|---|
| EIA | H | 811 | 768 |
| | V | 508 | 494 |




〔図3〕CCDインターライン転送方式

## 2-6-3. PA-147基板（XC-75）
## PA-152基板（XC-73）

カメラレンズを通してきた光は、PA基板のIC1（CCD）のチップ面に当たります。
CCD表面には、約40万個のフォトセンサー（感光素子）が配置されており、入射光は、フォトセンサー部で光の明暗に対応した電荷に変換されます。
変換された電荷は、設定された蓄積時間の間、フォトセンサーに蓄積された後、転送部に読み出されます。
転送部を順々に転送された電荷は、最終的にIC1の出力部に出力され、CCDとしての出力信号になります。
IC1からの出力信号は、Q3のバッファアンプを経て、IC2（CDS IC）に入力されます。
IC2では、相関2重サンプリングという処理によりCCD出力信号のノイズ成分が低減され、入力に対して約2倍のレベルで信号が出力されます。
IC2に入力されるSHP, SHDは、相関2重サンプリング用のサンプリングパルスです。
IC2から出力される信号は、Q1のバッファアンプを経てPA基板から出力され、MB-403基板に送られます。

## 2-6-4. MB-403基板

この基板には、CCD制御用のタイミングパルス発生回路の他、以下の回路部があります。

a. タイミングパルス発生回路
b. CCD垂直転送用クロックドライブ回路
c. 電子シャッター制御回路
d. CCD-VSUB電圧制御回路
e. PG-BIAS電圧制御回路
f. システムクロック発生回路
g. クロック出力用ドライバー
h. VIDEO信号出力用ドライバー

a. タイミングパルス発生回路

IC3は、システムクロック発生回路から28MHzのクロックを入力し、SG-199基板からHD, VD信号を入力することにより、CCDを駆動するために必要な各種タイミングパルスを発生します。
IC3により発生するタイミングパルスは、下記のとおりです。

| | |
|---|---|
| XPG | : CCDプリチャージゲート用クロック |
| XH1, XH2, XLH1 | : CCD水平転送用2相クロック |
| XV1～XV4 | : CCD垂直転送用2相クロック |
| XSUB | : 電子シャッター用パルス |
| XSG1, XSG2 | : フォトセンサーからの電荷読み出しパルス |

その他信号処理用のタイミングパルスを下記に示します。

| | |
|---|---|
| SH1 | : 相関2重サンプリング用サンプリングパルス |
| SH2 | : 相関2重サンプリング用サンプリングパルス |
| CLP3 | : 直流再生用クランプパルス |

ロータリーコードスイッチS1の出力に応じて発生期間を可変したシャッター用パルスX-SUBを出力し、電子シャッター制御回路に送ります。

b. CCD垂直転送用クロックドライブ回路

IC1は、IC3から送られてくるCCD垂直転送用クロックパルス（V1～V4）、および、フォトセンサーからの信号電荷読み出しパルス（SG1, SG2）を入力し、内部でSG1, SG2をV1, V3に付加した形でV1～V4パルスを出力します。

その際、IC1はCCDを直接駆動できるよう、V1～V4パルスのドライバーとして働きます。

さらに、V2出力は、D1, D2, C1, C2で構成されるチャージポンプ回路に送られ、ここでV-SUB用の直流電圧（約＋25V）を作成します。

c. 電子シャッター制御回路

IC4, 5, 6で構成される回路は、電子シャッターモード（NORMAL／SPECIAL）の切り換えおよび、SPECIALシャッターの制御を行っています。

JR1は工場出荷時点でOPENとなっていますが、この状態ではSPECIALシャッター用のIC6は、リセットされた状態になっています。一方、IC5で構成されるシャッターパルスの切り換え回路の出力は、NORMALシャッターパルスであるIC3出力のX-SUBが選択されています。

JR1をSHORTするとIC4の出力論理が反転して、IC6のリセットが解除されます。

そのとき、リアパネルの6Pコネクターからのトリガーパルスもしくはは VDに対して、動作可能となります。（VD／トリガーの選択は、ジャンパーランドJR2で行います。）

同時に、IC5で構成されるシャッターパルスの切り換え回路の出力は、IC6の出力パルスが選択され、これによりSPECIALシャッター動作が可能になります。

リアパネルの6Pコネクターから入力されるトリガーパルスはQ8の波形整形回路を通して、IC6に入力され、IC6は、Q8のコレクターに発生するパルスの立ち下がりを基準に、LASTシャッターパルスとシャッターOFFコントロールパルスの2つを出力します。

IC6の10番ピンから出力されたLASTシャッターパルスは、IC3からのXV2とIC5で合成され、6番ピンから出力されたシャッターOFFコントロールパルスで、出力期間を制限されて、SPECIALシャッター用パルスとしてIC1へ送られます。

d. CCD-VSUB電圧制御回路

Q12, 13, D6, 7, C1, 41, R45～51で構成される回路は、CCDのフォトセンサーをオーバーフローから防ぐために設けられたOFD（オーバーフロードレイン）に、各CCDで異なる適正直流電圧を与えるために、用意されたもので、TP1の値を読みながらRV1によって調整します。

Q12の3番ピンには、＋15 Vから作成された基準電圧（約＋5 V）が与えられており、Q12の5番ピンが、この電圧に平行するよう全体として動作します。D6の1番ピン側のダイオードは、シャッターパルスをTP1のDC電圧にクランプするためのクランプ用ダイオードで、D6の2番ピンのダイオードで1番ピン側のダイオードの温度補正をしています。

e. PG-BIAS電圧制御回路

R54, 55, C44, RV2で構成される回路は、CCDへ送るPGパルスの直流バイアスを調整するための回路で、TP2の値を読みながらRV2で調整します。

f. システムクロック発生回路

水晶発振部とL-C発振部で構成されています。

どちらの出力（28MHz）を選択するかは、自動で行われます。

カメラの外部から外部同期信号（HD／VDかVS）を入力するとSG-199基板のIC1（CXD-1084）の12番端子に“H”（＋5 V）が出力されます。このコントロール信号はMB-403基板のCN7の9番ピンに伝えられ、IC2の論理回路で構成されるスイッチ回路を制御します。その際、クロック出力としては、L-C発振部の出力が選択されIC3の入力へ送られます。

L-C発振部は、SG-199基板の一部の回路とPLLを構成しています。L-C発振部から出力された28MHzのクロックは、IC3で分周され14MHzのクロックとなってCN7の7番ピンを通してSG-199基板に送られ、SG-199基板のIC1へ入力されます。IC1では、このクロックをもとに、カメラの同期信号を作成していますが、外部同期時には外部同期信号から、水平同期の成分を分離したパルスH SEPを出力します。このパルスとクロックをもとに作成されたH REFは、位相比較器であるSG-199基板のIC2に入力され、それらの位相差成分がIC2から出力されます。

出力された位相差成分は、MB-403基板のCN7の10番ピンに送られ、MB-403基板のR39, C36, C39で構成されるローパスフィルターを通してD5のカソードに与えられます。
D5はバリキャップで与えられた電圧によって容量が変化するためIC2, R34, L6, C29, 30, 31, 43, CT1, D5で構成されるL-C発振回路の発振周波数が変化します。
ループとしては、クロックをもとに作成されたH REFと、外部同期信号から分離したH SEPの位相差が0となるようにH REFの位相を決めるクロックの発振を制御するよう構成されています。
CT1は、部品のバラツキを抑えるためのもので、規格中心の外部同期信号が入力したとき、PLLの可変範囲の中心値（D5のカソード電圧で＋2.5 V程度）で動作するよう設定します。
カメラの外部から外部同期信号が入力されていないときは、SG-199基板のIC1の12番端子に“L”（0 V）が出力されており、システムクロック発振部の出力はIC2の論理回路で構成されるスイッチにより、水晶発振部の出力が選択されています。

g. クロック出力用ドライバー
Q9, 10, 11, R40, 41, C38, 39で構成される回路は、B級バイアスプッシュプルタイプのケーブルドライバーで、特性インピーダンス75 Ωの同軸線をドライブすることができます。
IC3の57番端子から出力されたクロック（14MHz）は、この回路を通して、CN5の16番ピンに送られます。

h. VIDEO信号出力用ドライバー
PR-165基板で処理されたVIDEO信号は、CN1の6番ピンから入力され、Q14, R56, 57で構成されるバッファアンプに送られます。バッファを通った信号は、FL2, R59, 60で構成される14MHzトラップフィルターで14MHz成分のノイズを落して、出力ドライバー回路に入力されます。
出力ドライバー回路は、Q1～5, 7, R4～10, 15, 16, C6, 9, 11で構成されており、約1.7倍の電圧利得を持っています。
最終段は、プッシュプルタイプのケーブルドライバーとなっており特性インピーダンス75 Ωの同軸線をドライブすることができます。
VIDEO出力信号は、この回路を通してCN5の9番ピンに送られます。

## 2-6-5. PR-165基板

この基板は、CCDから得られたVIDEO信号のPROCESS処理を行う回路部があります。

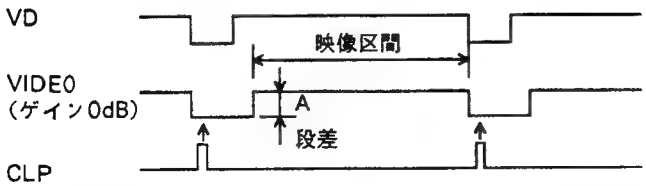
a. 固定ゲインアンプ
b. ブラックトラッキング用パルス作成回路
c. PROCESS IC
d. SYNC MIX回路

a. 固定ゲインアンプ

Q1, 3, 5, R10, 14～18, 21, 23, C8, 10で構成される回路は、約2倍の電圧利得を持ったアンプで、CN1の6番から入力するCDS処理された信号が入力されます。
この回路は、カメラのVIDEO出力信号として、高S/Nの信号を得るためのもので、リアパネルに配置されるGAINモードスイッチでFIXが選択されると、PR-165基板のVIDEO出力信号はIC2に内蔵されるアンプを通らずにPROCESS処理されて出力されます。
IC2に内蔵されるアンプは、電圧コントロールで利得が変化するタイプのアンプで、多くのトランジスタで構成されるため、信号がこの部分を通過すると、上記固定ゲインアンプに比べ、多少S/Nの劣化が見られます。
そこで、より高S/NのVIDEO信号を得るために、上記アンプが用意されています。

b. ブラックトラッキング用パルス作成回路

映像の黒レベルの変動を抑えるための回路です。
VIDEO信号は、PROCESS処理のため黒レベルがクランプパルスにより直流再生して、処理回路に入力されます。このとき、クランプ位相のレベルと映像の黒レベルとの間に多少の段差があった場合、VIDEOアンプ部でのゲインが変化すると、この段差が変動し、最終的には黒レベルの変動につながります。




上記のようにゲイン0 dBで、クランプ位相と映像の黒とのレベル差がAだけあった場合、クランプ位相のレベルが固定されているため、ゲイン6 dBでのレベル差はA×2となり黒レベルの浮きが大きくなってしまいます。

そこで、HD信号でアナログスイッチIC1をコントロールし、補正パルスを作成します。
作成された補正パルスはIC2と固定ゲインアンプに送られ、ゲインによる映像の黒レベルの変動がなくなるように、それぞれのVIDEO信号に加えられます。
補正パルスは、IC2とR4～9, C3, 6, 7, RV2, 3で構成される回路で作成します。補正レベルは、IC2用のパルスではRV2, 固定ゲイン用のパルスではRV3で設定します。

c. PROCESS IC

PROCESS ICの主な機能は、γ, WHITE CLIP, SET UPなどの信号処理と、AGC部で、他にAUTO IRISレンズ用に処理されたVIDEO信号も出力します。
CN1の6番ピンから入力したVIDEO信号は、Q2のバッファアンプを通して、IC2に入力されます。
IC2に入力した信号は、最初にアンプ部を通過して、いったんIC2から出力されます。
最初のアンプは電圧コントロールタイプのGAINコントロールアンプで、リアパネルのGAINモードスイッチがAUTOもしくはMANUALのとき、カメラ出力信号に対して有効になります。
リアパネルのGAINモードスイッチがAUTOもしくはMANUALのとき、CN2の3番ピンのCONT1信号は、"H"（+5 V）になりIC3のアナログスイッチの出力は、IC2のGAINアンプ出力を選択します。さらに、IC2の2番ピンのCONT2信号は、このGAINアンプのコントロール電圧の選択をしており、AUTO時は、IC2と外付け回路R27, 29, 33, 34, 37, 42, 43, C18, 19, 23, 25, Q7, RV9で構成されるAGCループの出力電圧が選択され、VIDEO信号の出力レベルは、入射光の変化に対して、自動的に一定レベルが保持される状態になります。VIDEO出力信号のレベルをどの程度に設定するかはRV9で調整します。また、最大ゲインの制限はRV10で行います。

一方MANUAL時はCOUNT2信号が“L”でGAINアンプのコントロール電圧として、CN2の1番ピンから入力されるコントロール電圧が選択されます。この電圧は、リアパネル側から操作できるボリュームにより、コントロールが可能で、GAINアンプのゲインは、このボリュームによりMANUALコントロールができるようになります。

リアパネルのスイッチにより、固定GAINアンプの出力か、IC2のGAINアンプの出力かを選択されたVIDEO信号はQ10のバッファアンプを通して再びIC2に入力されます。

IC2に入力されたVIDEO信号は、γ補正回路を通って出力される信号（GAM OUT）と、そのまま通過して出力される信号（LIN OUT）の2種類の信号を出力します。これらの信号は、JR1とJR2（又は、*S1）によって、γ：ONの場合は、GAM OUTか、γ：OFFの場合は、LIN OUTが選択され、Q6のバッファアンプを通して、再びＩＣ２に入力されます。

再びIC2に入力されたVIDEO信号は、SET UPおよびWHITE CLIPの設定がなされて、最終的にIC2から出力されます。

SET UPの設定は、RV1（γ：OFF）かRV4（γ：ON）によって行います。

一方、WHITE CLIPの設定は、RV5によって行います。

※PR-165基板の基板末尾が-11の場合はS1になります。

d. SYNC MIX回路

CN-2の5番ピンより入力されるSYNC信号は、RV8でレベル調整をされて、Q11のバッファアンプを通して、VIDEO信号にミックスされます。

一方、IC2でPROCESS処理されたVIDEO信号は、RV6によって適正レベルに調整されてCN2の6番ピンに送られ、PR-165基板から出力されます。

その他、IC2の27番端子からAUTO IRISレンズ用のVIDEO信号が出力されますが、この信号はQ9のバッファアンプを通してCN-2の4番ピンに送られ、PR-165基板から出力されます。

## 2-6-6. SG-199基板

SG-199基板は、MB基板とボードトウボードコネクタで結合されており、MB基板から送出されるクロックを受け入れ、これを基に各種同期信号を作成し、再びMB基板に送出するという役割を有しています。

SG-199基板上の回路を機能別に分類すると、次の4つのブロックに大別することができます。

a. 内部同期／外部同期選択ブロック
b. 各種同期信号発生ブロック
c. 機能設定ブロック
d. 位相比較ブロック

以下では、このブロック別に動作を説明します。

a．内部同期（“*I”）／外部同期（“*E”）選択ブロック

内部同期信号出力／外部同期信号入力を切り換えるスイッチがS1です。S1の設定により、S1の出力端子から、内部同期設定時は+5V、外部同期設定時は-9Vがコントロール電圧として送出されます。

※1 このコントロール電圧は、IC8，IC9のアナログスイッチで構成される垂直同期信号選択回路に入力されます。

また、HDの入力信号は直接S1によって切換えられます。

※ SG-199基板の末尾が-11と-12の場合は、[INT]および[EXT]で表示されています。

※1［SG-199基板の末尾が-11と-12の場合］
このコントロール電圧は、IC6，IC7のアナログスイッチで構成される水平同期信号選択回路、IC8，IC9のアナログスイッチで構成される垂直同期信号選択回路に入力されます。

内部同期信号出力

※2 S1を“*I”に設定すると、S1の出力端子から+5Vが送出されるため、IC9が「ON」、IC8が「OFF」となり、内部同期信号出力モードが選択されます。

同期信号発生回路であるIC1から出力されたHD信号は、S1に入力され、またVD信号は、アナログスイッチIC9に入力されます。VD信号のドライブ回路にはIC4が用いられていますが、HD信号については、入力されるアナログスイッチの抵抗、容量分によって生じるケーブル延長時の信号劣化を軽減するため、Q5、C24、R25、R26によって構成される回路が、ドライブ回路として用いられています。

アナログスイッチを経たHD信号、VD信号は、各々CN1の5pin、6pinから出力されます。内部同期信号出力を得るためには、外部同期信号終端用のスイッチS2,S3を「OFF」に設定して下さい。

HD信号およびVD信号は、SG基板からMB基板、CN基板を通り、リアパネルのコネクタよりカメラ外部へ出力されます。

※2 [SG-199基板の末尾が-11と-12の場合]
S1を"INT"に設定すると、S1の出力端子から+5Vが送出されるため、IC7、IC9が「ON」、IC6、IC8が「OFF」となり、内部同期信号出力モードが選択されます。
同期信号発生ICであるIC1から出力されたHD信号、VD信号は、それぞれドライブされてアナログスイッチIC7、IC9に入力されます。

● 外部同期信号入力

※3 S1を"*E"に設定すると、S1の出力端子から-9Vが送出されるため、IC8が「ON」、IC9が「OFF」となり、外部同期信号入力モードが選択されます。

外部同期動作を得るための、外部同期信号入力としては、

①HD信号／VD信号

②VSまたはSYNC信号

の2通りの信号が入力可能です。

※3 [SG-199基板の末尾が-11と-12の場合]
S1を"EXT"に設定すると、S1の出力端子から-9Vが送出されるため、IC6、IC8が「ON」、IC7、IC9が「OFF」となり、外部同期信号入力モードが選択されます。

①HD信号／VD信号同期モード

HD信号／VD信号同期モードでカメラを動作させたい場合には、リアパネルのコネクタからHD信号とVD信号を入力します。入力可能信号レベルは、いずれも2～5Vp－pです。入力されたHD信号、VD信号は、CN基板、MB基板を経て、各々CN1の5pin、6pinから入力されます。

ここで、外部から入力されたHD信号、VD信号を75Ωで終端したい場合には、外部同期信号終端用のスイッチS2、S3を、それぞれ「ON」に設定します。S2はHD信号、S3はVD信号に対応しています。75Ωで終端しない場合には、S2、S3を、それぞれ「OFF」に設定します。

※4 終端回路を経たHD信号は、Q2を中心に構成されている反転回路に入力されます。ここで、負極性のHD信号は反転されて正極性になり、レベルは4.5V程度になります。さらに、IC3のゲートを2段通り、波形整形され、約5Vp－pのレベルに整えられ、同期信号発生ICであるIC1に正極性で送られます。IC3のゲートのうち、2段目のゲートはスイッチの役割を有しています。HD信号とVD信号が同時に入力されず、HD信号のみが入力された場合、不適状態を検出し、このゲートが「OFF」となり、HD信号を送出しないように働きます。

一方、VD信号については、終端回路を経たあと、アナログスイッチIC8を経て、Q1、Q3を中心に構成されている同期信号分離回路に入力され、約4Vp－pのレベルになります。さらに、IC3のゲートを2段通り、波形整形され、約5Vp－pのレベルに整えられ、同期信号発生ICであるIC1に負極性で送られます。

※4 [SG-199基板の末尾が-11と-12の場合]
終端回路を経たHD信号は、アナログスイッチIC6を経て、Q2を中心に構成されている反転回路に入力されます。

②VSまたはSYNC信号同期モード

VSまたはSYNC信号同期モードでカメラを動作させたい場合には、リアパネルのコネクタからVSまたはSYNC信号を入力します。入力可能信号レベルは、SYNC信号レベルで0.3+0.3-0.15Vp－pです。入力されたVSまたはSYNC信号は、CN基板、MB基板を経て、CN1の6pinから入力されます。

ここで、外部から入力されたVSまたはSYNC信号を75Ωで終端したい場合には、外部同期信号終端用のスイッチS3を「ON」に設定します。75Ωで終端しない場合には「OFF」に設定します。

終端回路を経たVSまたはSYNC信号は、アナログスイッチIC8を経て、Q1、Q3を中心に構成されている同期信号分離回路に入力されます。ここで、VS信号の場合には、この回路でVS信号から同期信号だけが分離され、同期信号のみが約4Vp－pのレベルで送出されます。また、SYNC信号の場合には、波形はそのままで、約4Vp－pのレベルで送出されます。これらの同期信号は、さらに、IC3のゲートを2段通り、波形整形され、約5Vp－pのレベルに整えられ、同期信号発生ICであるIC1に負極性で送られます。

b. 各種同期信号発生ブロック

IC1を中心とする回路ブロックは、各種同期信号発生回路ブロックです。MB基板のタイミング発生ICが出力する14MHzのクロックは、CN1の7pinを経て、IC1に入力されます。IC1では、このクロックに基づいて、次に示すような、カメラを動作させるのに必要な各種同期信号を作成します。

HD　：水平同期信号
VD　：垂直同期信号
SYNC：コンポジットシンク信号

BLKG　：ブランキング信号
FLD　：フィールド識別信号
INT／EXT　：同期モード切り換え信号
内部同期モード時…“L”レベル
外部同期モード時…“H”レベル

IC1の内部では、内部同期／外部同期を自動検出しており、IC1のEXT　HD端子、EXT　VD端子に、1024ライン期間以上所定の信号が入力されない場合には、自動的に内部同期モードになります。

したがって、特殊シャッター等を使用していないノーマル動作モードの場合には、S1の設定が「*E」になっていても、上述のように、一定期間内に信号入力がないと、内部同期モード動作となります。

カメラの同期モードが、内部同期になっているか、外部同期になっているかの情報は、同期モード切り換え信号としてIC1より出力されます。内部同期モード時には“L”レベル、外部同期モード時には“H”レベルが、IC1からCN1の9pinを経て、MB基板に出力され、クロックの発生源である発振回路の選択を行います。

また、BLKG信号については、映像信号の品位に悪影響を及ぼさないように、出力部にD1、C4、R17、R19によって構成されるスパイクフィルタが設けられており、特に注意が払われています。

*2-32 (J) 参照

c.　機能設定ブロック

同期信号発生ICであるIC1は多彩な機能を有しています。これらの機能の選択は、所定の入力端子に、設定すべきモードに応じて“H”レベル、または“L”レベルの電圧を入力することにより設定することができます。本カメラでは、これらの機能設定用として、ジャンパーランド（JR1～JR9）を設けています。これらのジャンパーランドを、設定すべきモードに応じて、「OPEN」または「SHORT」させることにより、機能を設定することができます。

JR1～JR9のジャンパーランドは、各々、以下の機能に対応しています。

JR1～JR6　：外部水平同期信号位相進相量
JR7・JR8　：リスタート　リセット／ノーマルモード選択
JR9　：フィールド　インバート／ノーマルモード選択

各々の機能の詳細については、2-5. 動作モードの設定と機能に記載されています。該当する項目を参照して下さい。

d.　位相比較ブロック

IC2を中心とするブロックは位相比較ブロックです。IC1から出力されるH REF信号とH SEP信号を受け取り、位相比較を行います。

内部同期モード時には、H SEPが固定出力となり、位相比較回路は動作しません。外部同期モード時には、場合に応じて次の信号が、IC1よりH SEPとして出力されます。HD信号／VD信号同期モード時には、入力された信号の水平同期信号成分がそのまま出力されます。VSまたはSYNC信号同期モード時には、IC1内において、入力されたVSまたはSYNC信号から水平同期成分が分離され、これが出力されることになります。

一方、H REFは、IC1内で作成されるHD信号を基準にして作られます。IC1内では、MB基板から入力されるクロック信号に基づいてHD信号が作られています。H REFには、このHD信号に対して、機能設定により規定される量だけ位相を遅延させた信号が出力されます。すなわち、H REF信号とHD信号の位相関係は、HD信号を基準にして考えると、H REFは、HD信号よりも設定量の分だけ位相が遅相しているといえます。また、見方を変えてH REFを基準にして考えると、HD信号は、H REFを、設定量だけ位相を進相させたものであると言うこともできます。

以上述べたように、外部から入力される水平同期信号から作られているのがH SEP信号であり、内部クロック信号から作られているのがH REFであります。正しい外部同期動作を得るには、カメラの動作クロック位相を、外部から入力される水平同期位相に合わせる必要があります。そのため、IC2では、IC1から送られてくる、H SEP信号とH REF信号の位相比較を行い、これらの信号の位相差を0にするには、H REFを進ませるべきか、遅らせるべきかを判断し、この結果を、コントロールパルスの極性の正・負として出力します。このコントロールパルスは、CN1の10pinを経て、MB基板に入力され、DC電圧に変換されて電圧制御型発振回路（VCO）に入力され、クロック周波数を制御します。このループにより、H SEP信号とH REF信号の位相差が常に0になるように制御されているため、外部から入力される同期信号の周波数偏差が、基準水平同期周波数に対して±1%以内であれば、カメラを正常に動作させることが可能です。

## 2-6-7. PS-268基板

PS-268基板は、MB基板とボードトウボードコネクタで結合されています。この基板は、機能面から言えばDC電源発生基板であると言えます。PS-268基板は、MB基板を始め、MB基板を通じて全ての基板に対して、各回路の動作に必要なDC電源を供給する役割を有しています。

この基板の中心になっているのは、DC/DCコンバータPU1であります。このD/Dコンは、XC-75/73シリーズの小型化、および省消費電力化を実現するために、新規に設計したものです。そのため、外形寸法、電気的特性等、XC-75/73シリーズのカメラが要求する仕様に合わせて設計されています。

D/DコンPU1を正常に動作させるため、カメラの電源電圧の基準入力電圧は、Vin = 12.0 V、動作保証電圧範囲は、Vin = 10.5~15.0 Vに設定されています。この入力電源電圧は、リアパネルのコネクタからCN基板、MB基板を経て、PS基板のCN1の1、2pinに入力されることになります。D/Dコンの入力電圧端子UNREG INに適切な電源電圧が印加されますと、出力端子からは、-9 V、+5 V、+15 Vという3系統の出力電圧が得られます。これらの出力のうち、+5 V出力は、PS基板上で2系統に分けられます。一方はアナログ系専用に供給され、もう一方はディジタル系専用に供給されます。このように、+5 V出力を2分することにより、ノイズ等の発生によってもたらされる5 Vライン間相互の悪影響を防いでおり、回路誤動作や信号品位の劣化を抑えています。これらの出力は、全基板に、各回路の必要に応じて、DC電源や基準電圧として供給されており、それぞれの用途に適した電圧値が利用されています。

しかし、D/Dコンから出力される3種の電圧値では、性能が十分に発揮できない回路や、他の電圧値の電圧供給が必要不可欠な回路もあり、各基板には、必要に応じて、電圧レギュレータ回路が設けられている箇所もあります。PS基板には、Q101、Q102を中心に、-9 V出力から-5 Vを作り出すレギュレータ回路が構成されています。

これは、MB基板上にあるビデオ信号ドライブ回路に-5 Vを供給するための回路であります。このビデオ信号ドライブ回路は、カメラの映像出力をドライブしており、特に重要な回路であるため、PS基板上で作られた-5 V電源が専用で使われております。

## 2-6-8. CN-649基板

CN-649基板は、リアパネルに取り付けられている小基板であり、MB基板とフレキシブル基板で結合されています。

CN-649基板には、12pinマチコネクタ、6pinコネクタ、BNCコネクタ、ゲイン設定切り換えスイッチ、マニュアル ゲイン ボリュームなどが実装されています。CN基板は、主に、これらの外部入出力コネクタ、ゲイン設定用スイッチ、ボリュームとMB基板との中継基板の役割を有しています。

以下では、機能別に順を追って動作を説明していくことにします。

a. 入出力コネクタ

CN1は、12pinマルチコネクタです。このコネクタには、DC IN端子があり、カメラを動作させるのに必要なDC電源（+12 V）は、ここから供給されます。CN基板に入力された電源は、直ちにヒューズF1を通ります。これにより、異常な電源が接続された場合でも、このヒューズが切れるため、カメラ本体の破壊を防ぐことができます。DC電源は、CN基板から、MB基板を経てPS基板に送られ、カメラを動作させるのに必要なDC電源に変換されます。

適切な電源を供給することにより、MB基板からCN基板にビデオ出力信号が送出されます。CN基板に入力されたビデオ出力信号は、クロックによって生じる14MHz成分のノイズを除去するため、14MHzのトラップ回路を経て、CN1の4pin、およびCN3のBNCコネクタから出力されます。

CN1には、HD信号端子6pin、VD/SYNC信号端子7pinがありますが、これらのピンは、同期モードによって、入出力設定が異なります。

本カメラに、同期信号発生器を接続して、外部同期信号を入力することにより、カメラを外部同期で動作させることができます。外部同期動作時には、所望の外部同期モードに応じて、下表に示されている信号を、CN1の6pin、7pinから入力します。

| ピン番号 | 外部同期モード | | |
|---|---|---|---|
| | HD/VD | VSまたはSYNC | リスタートリセット |
| 6 | HD信号 | ―――― | HD信号 |
| 7 | VD信号 | VSまたはSYNC信号 | リセット信号 |

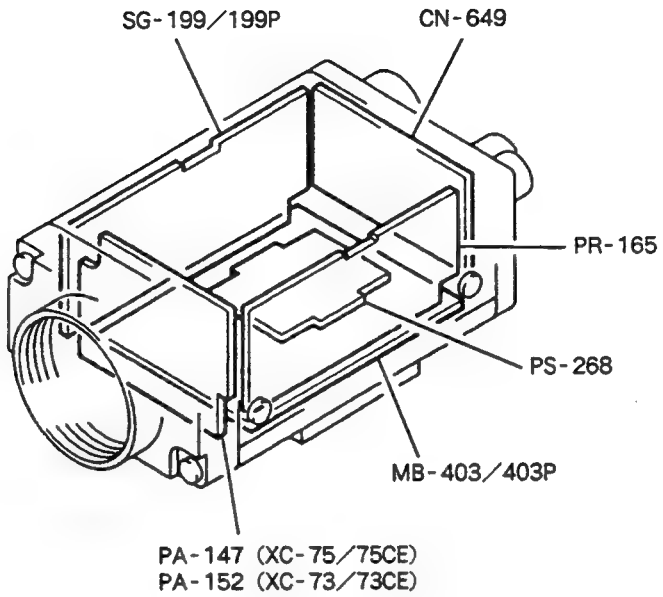
一方、内部同期時には、SG基板上のスイッチの設定により、CN1の6pin、7pinから、それぞれHD信号、VD信号を出力させることができます。
さらに、CN1からクロック信号を出力させることができます。CN基板上のジャンパーランドJR1は、通常「OPEN」となっていますが、これを「SHORT」することにより、CN1の9pinからクロック信号が出力されます。
CN2は、6Pコネクタです。一般に、このコネクタには、オートアイリスレンズが接続されます。
PR基板から出力されるオートアイリスレンズ用ビデオ信号は、MB基板を経て、CN基板に入力され、ローパスフィルタを通りCN2の5pinから出力されます。オートアイリスレンズの絞りは、この信号により自動調整させます。
また、オートアイリスレンズ用の電源（DC：＋12 V）は、CN2の6pinより出力されます。
他にも、CN2には、特殊用途にも対応できるよう、次の端子が設けられています。
1pinはフィールド識別信号出力端子になっています。カメラがノンインターレスモードで動作している場合に、ODDフィールド走査動作時には“H”レベルが、EVENフィールド走査動作時には“L”レベルが、フィールド識別信号としてSG基板から出力されます。この信号が、SG基板からMB基板を経てCN基板に入力され、ローパスフィルタを通りCN2の1pinから出力されます。
2pinはトリガー信号入力端子になっています。特殊電子シャッター設定時において、露光スタートのタイミングを外部からコントロールしたい場合に、この端子からトリガー信号を入力します。
入力信号条件、シャッター動作等の詳細については、2-5. 動作モードの設定と機能に記載されています。該当する項目を参照して下さい。

b. ゲイン設定スイッチ・ボリューム

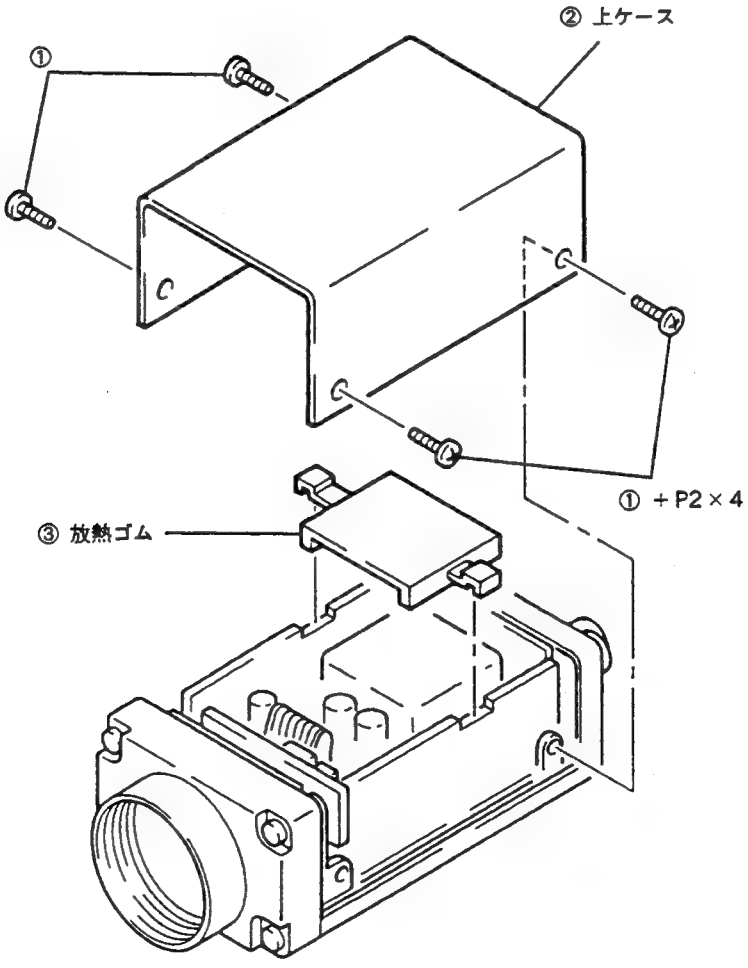
S1は、ゲイン設定切り換えスイッチになっています。このスイッチにより、ビデオ出力信号のゲイン（利得）を設定します。
ゲイン設定には、AGC（自動調整）、FIX（固定）、MANU（手動調整）の3通りのモードがあり、これらの中から、S1により所望するモードを選択します。
S1には、出力端子が2端子あり、“H”レベル、または“L”レベルのいずれかの電圧が、設定モードに応じてS1により選択されて、コントロール電圧として出力されます。このコントロール電圧は、設定モード毎に、2系統の出力レベルの組み合わせが異なるように設計されています。そのため、この電圧を受けるPR基板では、CN基板からMB基板を経て送られてくるコントロール電圧によって、ゲインモードを判断することができます。コントロール電圧は、PR基板内のアナログスイッチに、コントロール信号として入力され、設定されたゲインモードでカメラが動作するように、スイッチを切り換えています。
3通りのモードの内、MANU（手動調整）ゲインモード時には、マニュアルゲインボリュームRV1により、0 dB～＋18 dBの範囲内の希望するゲインに、カメラのゲインを手動調整することができます。RV1により、希望するゲインに応じた電圧値がCN基板から出力され、MB基板を経てPR基板内の信号発生ICに送られ、ビデオ信号アンプのゲインを制御しています。

# 第3章
# サービスインフォメーション

## 3-1. 基板配置図

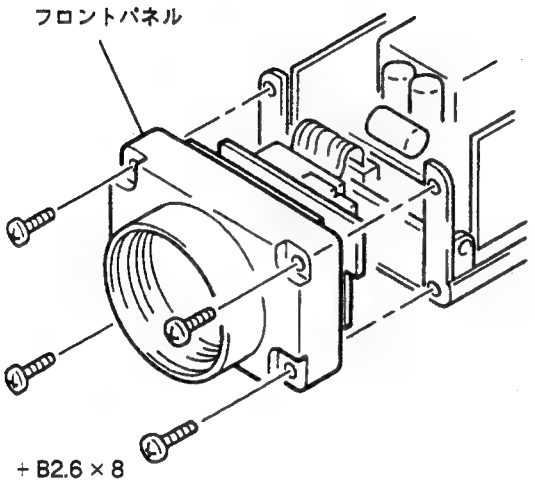



## 3-2. 外装の外し方

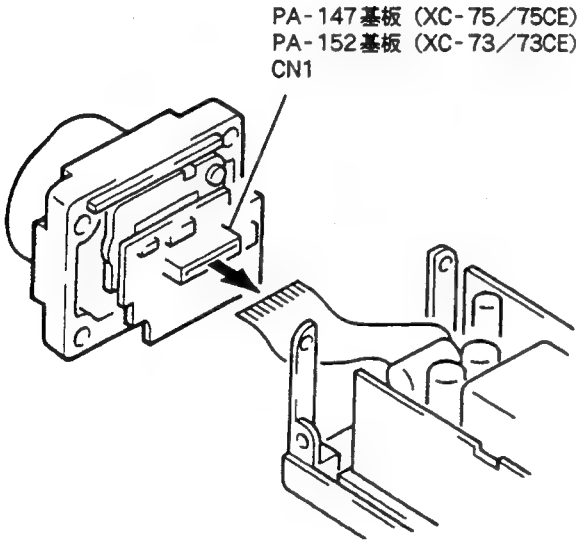


## 3-3. CCDユニットの交換方法

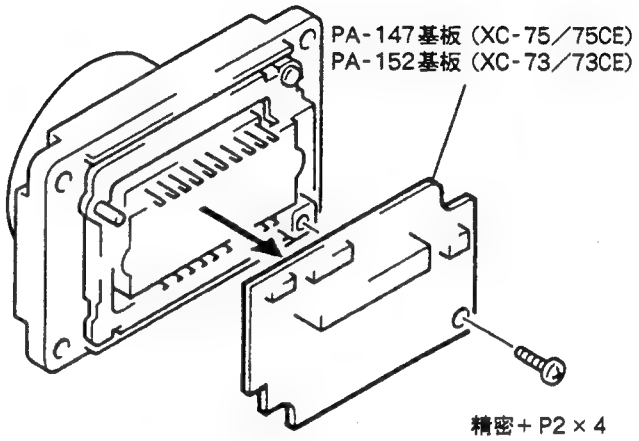
1. “3-2. 外装の外し方”を参照し、上ケースを外します。
2. フロントパネルを本体にとめているねじ4本（+B2.6×8）を外します。




3. PA基板のCN1を外します。




4. ねじ1本（精密+P2×4）を外し、PA基板の半田を外します。



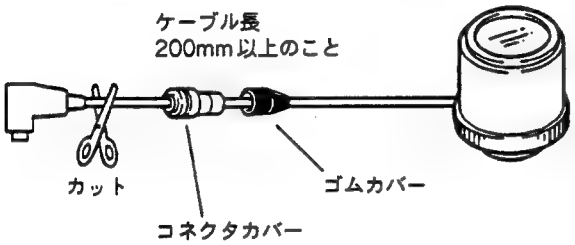

5. CCDユニットを新しい物と交換します。組み立ては取り外しと逆の手順で行います。
6. CCDユニットの交換後は、第4章の調整要項を参照の上、調整を行って下さい。

## 3-4. オートアイリスレンズ改造方法

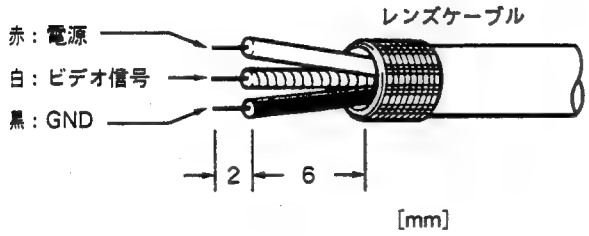
構成

- オートアイリスレンズ　VCL-16Y
- 6pinコネクタ　PC-XC06

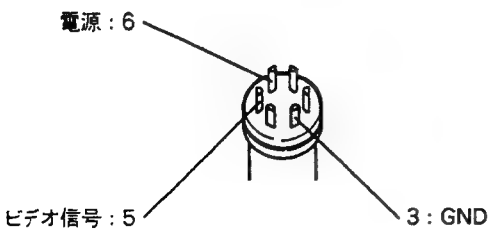
1. オートアイリスレンズVCL-16Yのレンズケーブルをケーブル長が200mm以上になるようにカットし、6pinコネクタPC-XC06のゴムカバー及びコネクタカバーを予め挿入しておく。



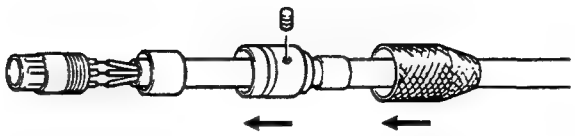

2. ケーブルの芯線を処理する。
6本の芯線のうち、必要な3本のみ（赤、白、黒）を残し、不要な3本は切断する。編組線は折り返しておく。




3. 6pinコネクタのピンに半田付けをする。

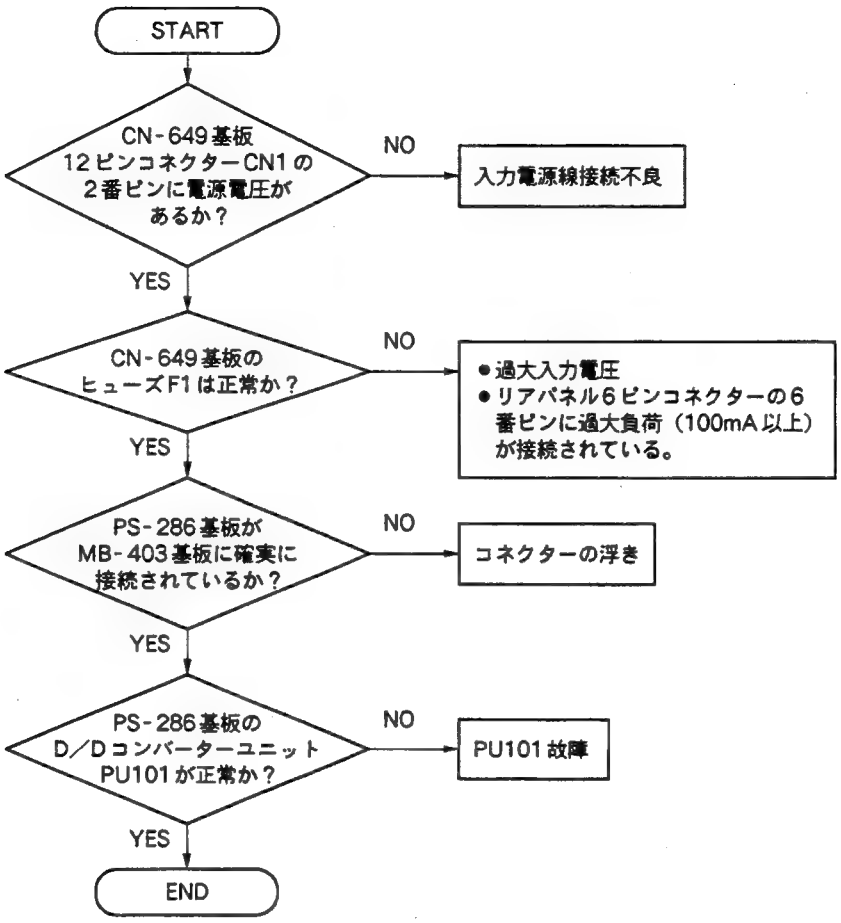



4. 編組線の折り返し部に6pinコネクタ付属のアース金具を巻き付けコネクタカバーをかぶせロックねじで固定し、さらにゴムカバーをかぶせる。

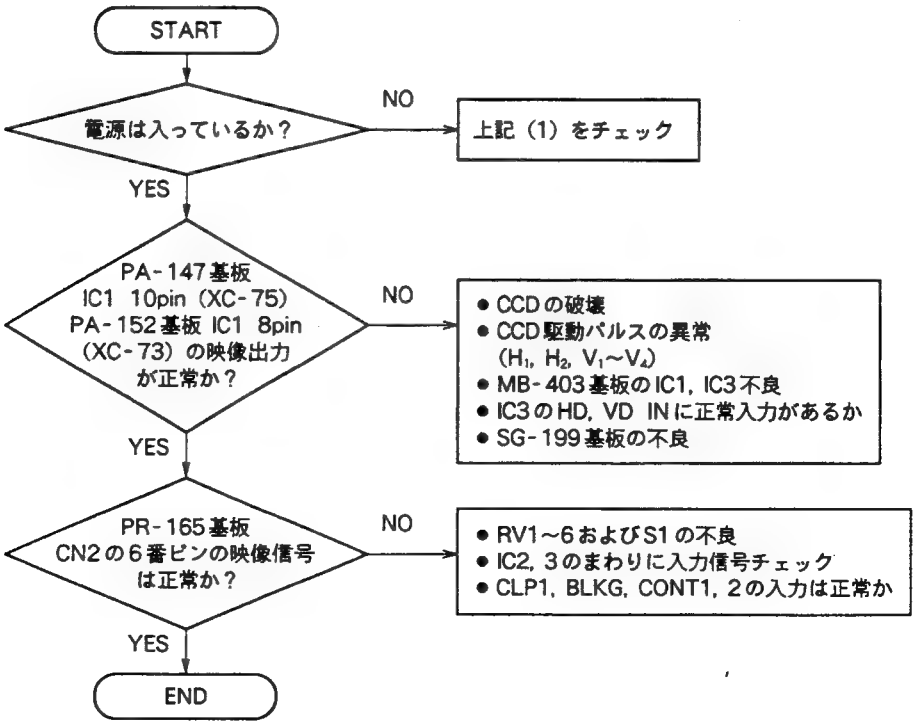


## 3-5. トラブルシューティング

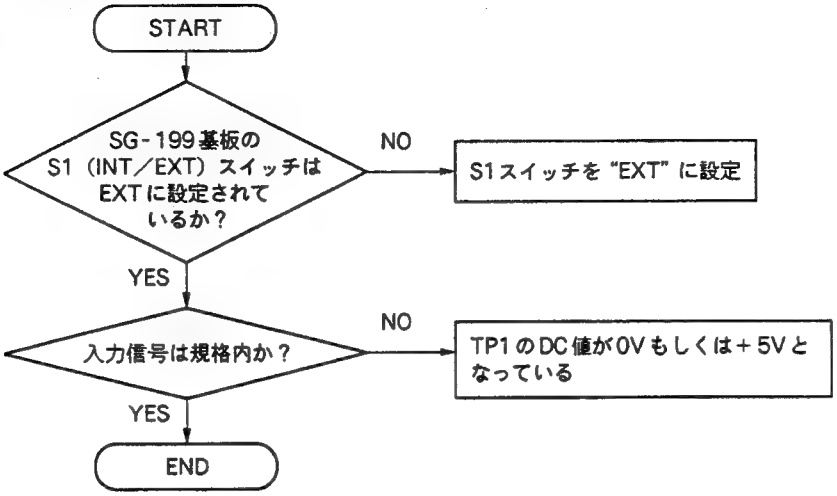
(1) 電源が入らない場合



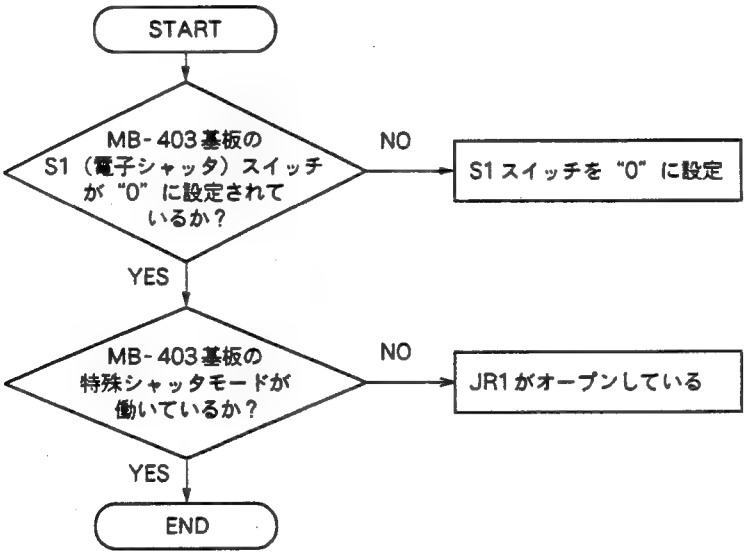

(2) 画像が出ない場合



(3) 外部同期がかからない場合




(4) 出力画像が異常に暗い場合

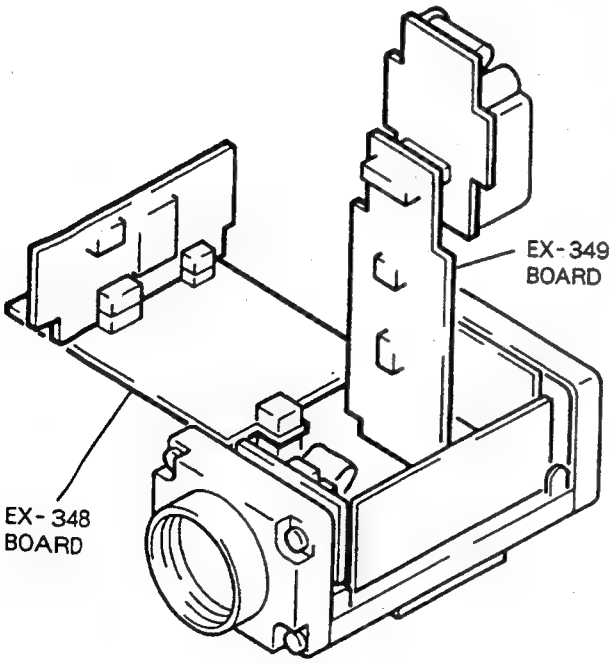


# 第4章
# 調整要項

## 4-1. 準備

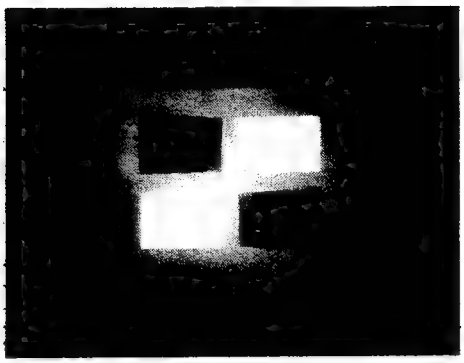
### 4-1-1. 使用機器

- ●オシロスコープ
- ●波形モニター
- ●白黒モニター
- ●デジタル電圧計
- ●電源供給用機器
- ●ジャンクションボックスJB-77（市販品）および安定化電源
- ●電流計
- ● HD／VD信号発生機（Shibasoku TG-7）
- ●周波数カウンター
- ●三脚アタッチメントVCT-37（市販品）
- ●レンズ　標準：VCL-12YM（市販品）（XC-75）
  VCL-08YM（市販品）（XC-73）
- ●パターンボックスPTB-500またはPTM-100
  ソニー部品番号J-6029-140-A
- ●延長基板EX-348
  ソニー部品番号J-6096-750-A
- ●延長基板EX-349
  ソニー部品番号J-6096-760-A



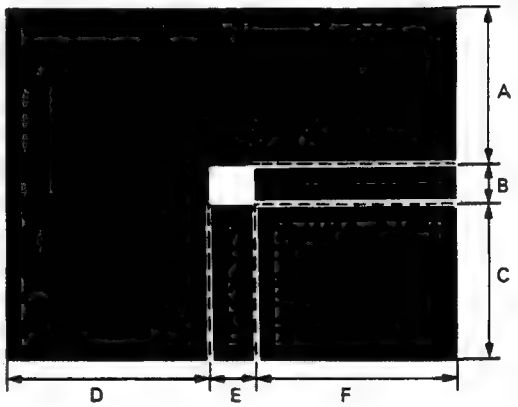

基板延長の方法

- ●グレースケールチャート
  ソニー部品番号J-6026-130-A



- ● NDフィルター（50％ Transmittance）

- ●ウインドウチャート
  黒い紙に図のように穴を開ける。
  ウインドウ部に透過率10 ％のNDフィルタを貼る。

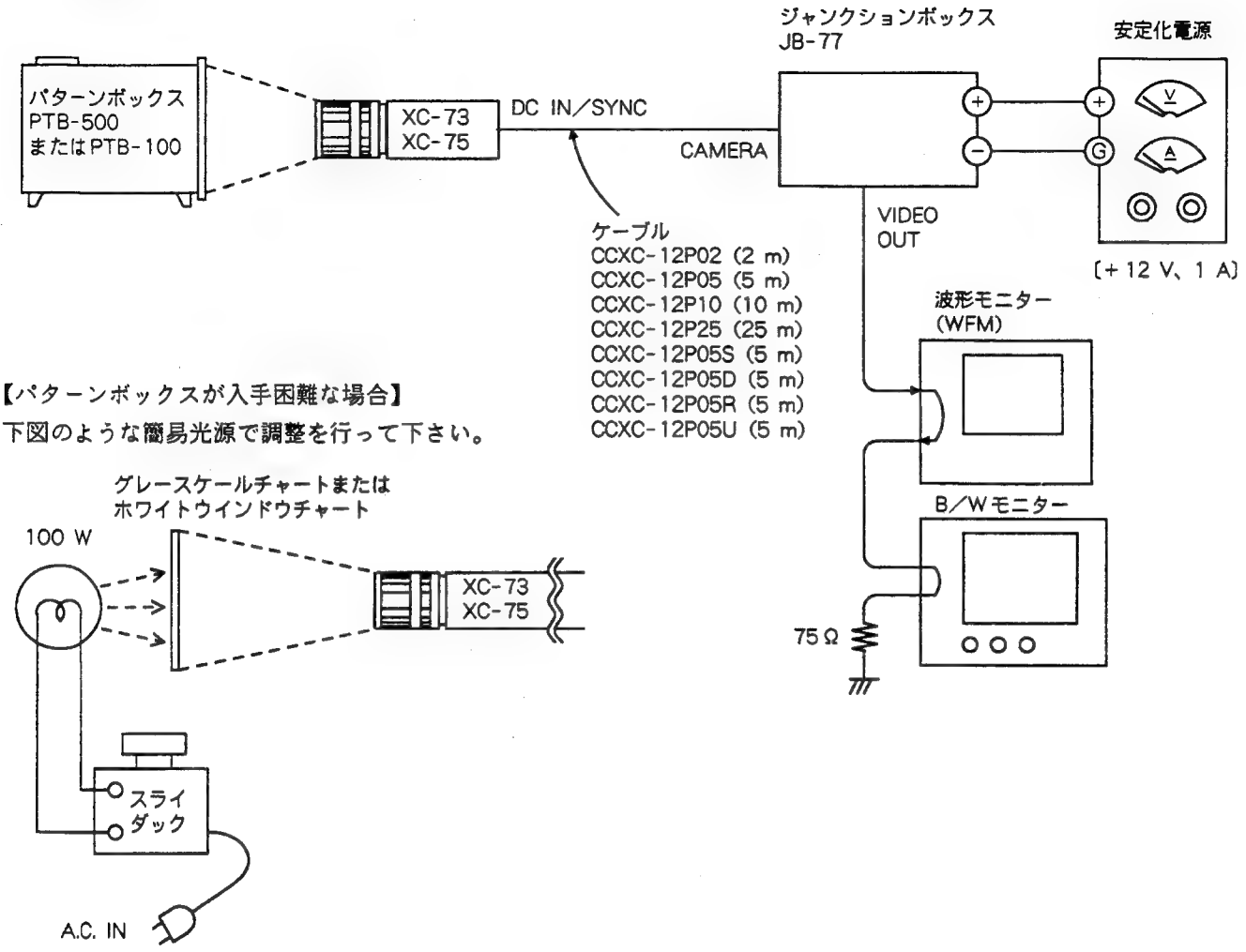



Vertical A:B:C = 4.5:1:4.5
Horizontal D:E:F = 4.5:1:4.5

【パターンボックスが入手困難な場合】

- ●電球100 W
- ●スライダック

4-1-2. 接続図




4-1-3. 水晶発振子周波数確認

1. 延長基板EX-348/349を使用して、SG-199基板及びPS-268基板を延長します。(4-1-1. 使用機器参照)
2. POWERスイッチをONにします。
3. 周波数カウンタを7ピン/延長基板EX-348に接続します。表示が規格Aを満足することを確認します。

$$A = 14.31818 \pm 0.001 \text{ MHz}$$

4. 規格を満足しない場合、MB-403基板のC45を次のいずれかに交換してください。

| | | |
|---|---|---|
| C45 | 1pF | 1-162-905-11 |
| | 2pF | 1-162-907-11 |
| | 3pF | 1-162-908-11 |

## 4-2. 総合調整

ステップ1. V RGL、V SUB電圧調整

調整を始める前に：

S1／SG-199基板　→EXT
S2／SG-199基板　→OFF
S3／SG-199基板　→OFF

注意事項

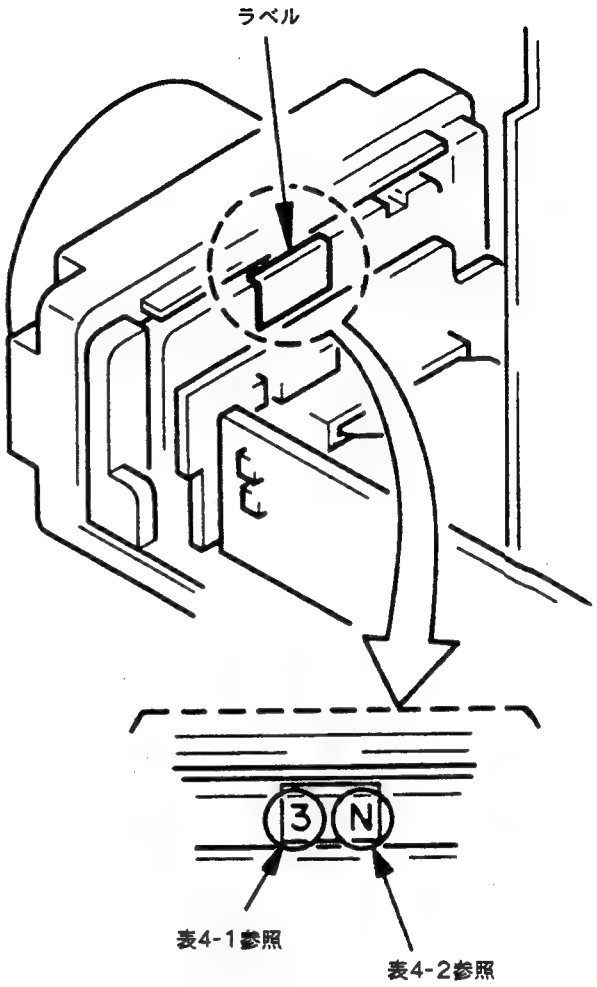
CCDを交換した場合以外は絶対にこの調整を行わないで下さい。

デジタル電圧計のGNDはシャーシ等から取って下さい。

測定器：　デジタル電圧計
測定点：　TP1／MB-403基板
　　TP2／MB-403基板
調整箇所：◐RV1／MB-403基板
　　◐RV2／MB-403基板

調整手順

1. セット上に貼添されたラベルの値を表4-1、表4-2と参照しV RGL、V SUBの調整電圧を確認する。
2. TP1にデジタル電圧計を接続し◐RV1／MB-403基板にて表4-2で参照した電圧にV SUB電圧を調整する。
3. TP2にデジタル電圧計を接続し◐RV2／MB-403基板にて表4-1で参照した電圧にV RGL電圧を調整する。




| ① | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| 数値 | 1.0 | 1.5 | 2.0 | 2.5 | 3.0 | 3.5 | 4.0 |

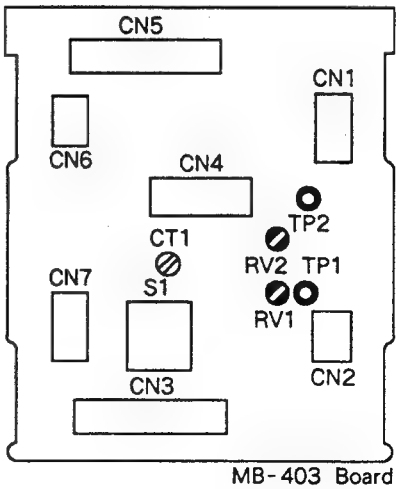
（単位：V）

表4-1：V RGL電圧

| ② | E | f | G | h | J | K | L |
|---|---|---|---|---|---|---|---|
| 数値 | 9.0 | 9.5 | 10.0 | 10.5 | 11.0 | 11.5 | 12.0 |
| ② | m | N | P | Q | R | S | T |
| 数値 | 12.5 | 13.0 | 13.5 | 14.0 | 14.5 | 15.0 | 15.5 |
| ② | U | V | W | X | Y | Z | |
| 数値 | 16.0 | 16.5 | 17.0 | 17.5 | 18.0 | 18.5 | |

（単位：V）

表4-2：V SUB電圧




MB-403 Board
－B Side－

## ステップ2. VCO電圧調整

測定器： デジタル電圧計
測定点： TP1／SG-199基板
調整箇所：●CT1／MB-403基板
規格： 2.5 ± 0.1 V

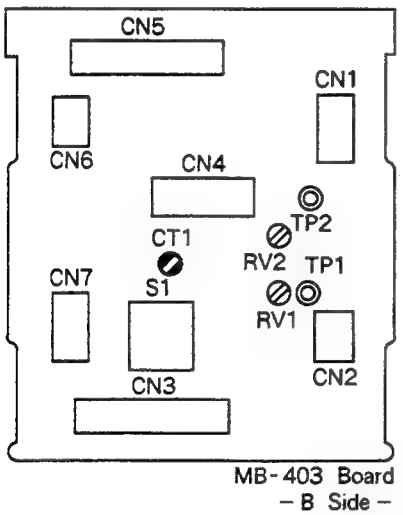
調整手順

1. JB-77のHD／VD入力端子に信号発生器にて所定の信号を入力する。(表4-3参照)
2. ●CT1／MB-403基板にてTP1／SG-199基板のDCレベルが2.5 ± 0.1 Vとなるように調整する。
3. 電源スイッチをOFFにし、延長基板を取り外し、PS-268基板、SG-199基板を直接MB-403基板に取付ける。
4. 電源スイッチをONにする。

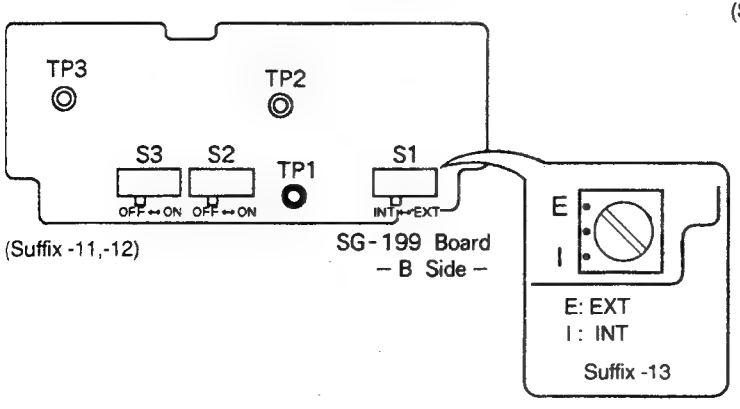
| 入力端子 | HD | VD |
|---|---|---|
| 周波数 | 15.734 kHz | 525 fH／2 |

注意：VD, HDともに入力レベルは$V_{IN}$ = 2.0～5.0 V p-p

表4-3




MB-403 Board
– B Side –



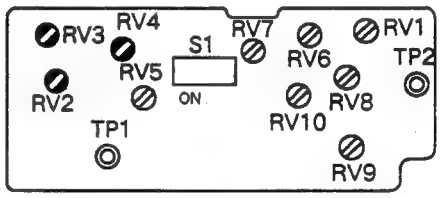

(Suffix -11,-12) SG-199 Board – B Side –

Suffix -13

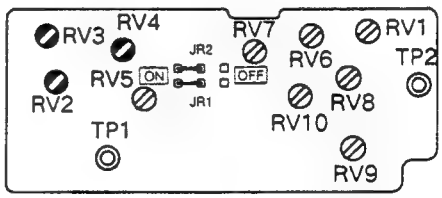
## ステップ3. BLACK TRACKING調整

注意事項
ステップ3. BLACK TRACKING調整からステップ4. PEDESTALレベル仮調整までの調整は連続して行います。

測定器： オシロスコープ
波形モニター
測定点： TP2／PR-165基板
VIDEO OUT端子／リアパネル
調整箇所：●RV2／PR-165基板
●RV3／PR-165基板
●RV4／PR-165基板
規格： 段差A < ± 2 mV
準備： レンズ → クローズ
GAINスイッチ／リアパネル → M
※S1／PR-165基板 (基板末尾 -11) → ON
※JR1, JR2／PR-165基板 (基板末尾 -12) → ON
※基板末尾によって異なります。



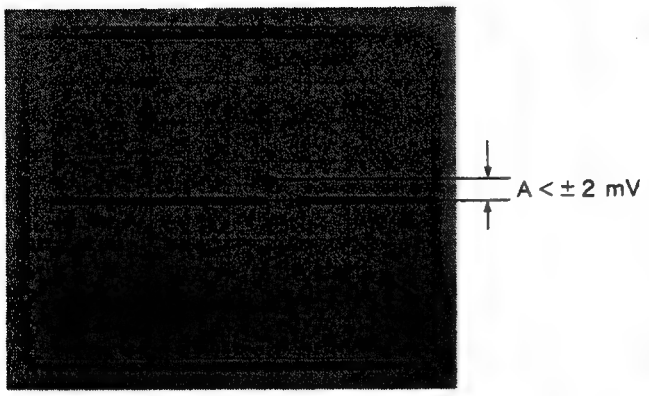

(Suffix -11) PR-165 Board – B Side –

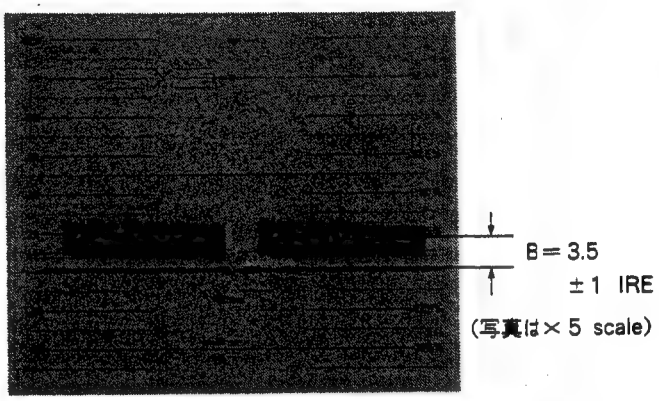



(Suffix -12) PR-165 Board – B Side –

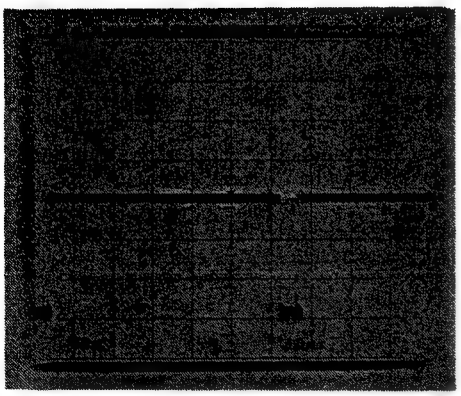
調整手順

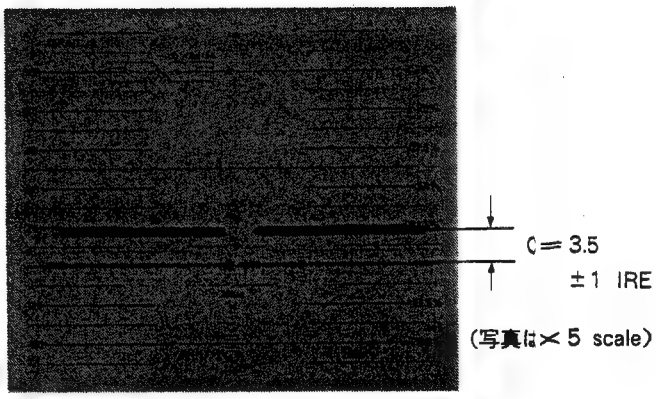
1. GAINボリューム／リアパネルを左右一杯に回したとき、オシロスコープにて波形を確認し、段差Aが最小になるように◐RV2／PR-165基板を調整する。
2. GAINスイッチ／リアパネルをFにする。
3. GAINボリューム／リアパネルを左右一杯に回したとき、段差Aが最小になるように◐RV3／PR-165基板を調整する。
4. GAINスイッチ／リアパネルをMにする。
5. VIDEO OUTのペデスタルを波形モニターで確認し◐RV4／PR-165基板にてペデスタルレベルが3.5±1 IREになるように調整する。（SCALE×5にすると変化が読み取りやすくなります）
6. GAINボリューム／リアパネルを左右一杯に回したとき、VIDEO OUTのペデスタルレベルの変動が最小になるように◐RV2／PR-165基板を調整する。
7. リアパネルのGAINボリュームをMINIMUM（↺）にする。




(GAIN : MAX)






(GAIN : MINIMUM)

B-C : MINIMUM

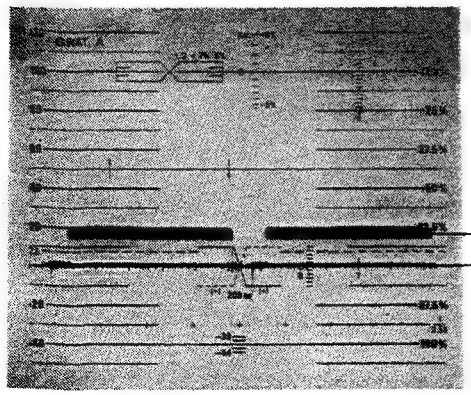
## ステップ4. PEDESTAL仮調整

注意事項
この調整を行う前にステップ3. BLACK TRACKING調整を済ませて下さい。

測定器： 波形モニター
測定点： VIDEO OUT端子／リアパネル
調整箇所：◐RV1／PR-165基板
◐RV3／PR-165基板
◐RV4／PR-165基板
規格： 段差A＝3.5±1 IRE
準備： レンズ → クローズ
GAINスイッチ／リアパネル → M
※S1／PR-165基板 (基板末尾-11) → ON
※JR1, JR2／PR-165基板 (基板末尾-12) → ON
※基板末尾によって異なります。

調整手順
(波形モニターのSCALE×5にすると変化を読み取りやすくなります。)

1. ◐RV4／PR-165基板にて下図のA＝3.5±1 IREになるように調整する。
2. GAINスイッチ／リアパネルをFにする。
3. ◐RV3／PR-165基板にて下図のA＝3.5±1 IREになるように調整する。
4. GAINスイッチ／リアパネルをMにする。
5. S1／PR-165基板をOFFにする。
6. ◐RV1／PR-165基板にて下図のA＝3.5±1 IREになるように調整する。
7. GAINスイッチ／リアパネルをFにする。
8. 波形モニターにて下図のA＝3.5±1 IREである事を確認する。



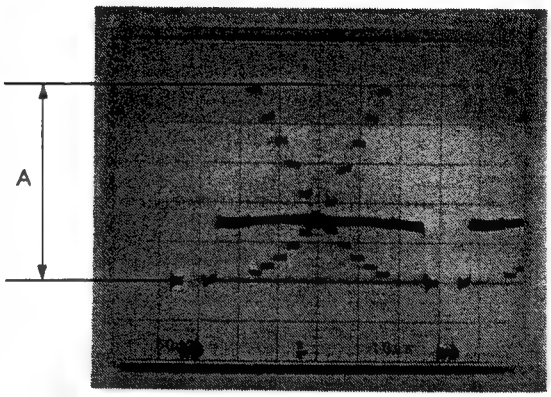
(写真は×5 scale)

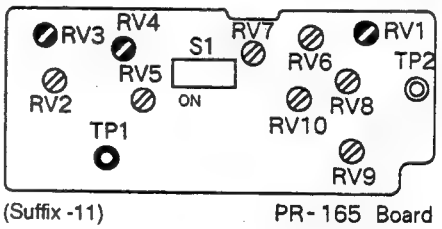
## ステップ5. 基準入力調整

測定器： オシロスコープ
被写体： グレースケールチャート
測定点： TP1／PR-165基板
調整箇所：レンズ絞り
準備： ※S1／PR-165基板 (基板末尾-11) → ON
※JR1, JR2／PR-165基板 (基板末尾-12) → ON
※基板末尾によって異なります。
◐RV5が下図の位置になっている事を確認する

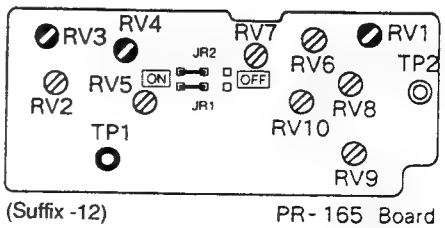

(◐RV5上面図)

規格： A＝250±10 mV



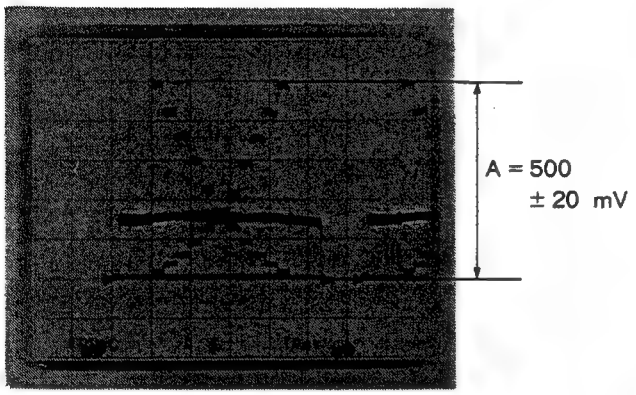
(Suffix -11) PR-165 Board
－B Side－



(Suffix -12) PR-165 Board
－B Side－

## ステップ6. VIDEOレベル調整（1）

測定器： オシロスコープ
被写体： グレースケールチャート
測定点： TP2／PR-165基板
調整箇所：◐GAINボリューム／リアパネル
準備： GAINスイッチ／リアパネル → M
※S1／PR-165基板（基板末尾-11） → ON
※JR1, JR2／PR-165基板（基板末尾-12） → ON
*基板末尾によって異なります。
規格： A＝500±20 mV

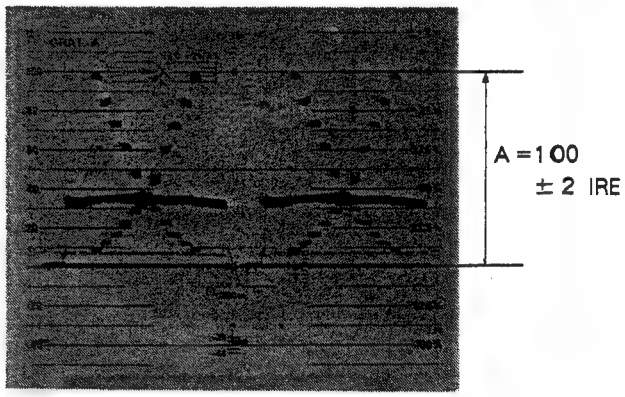


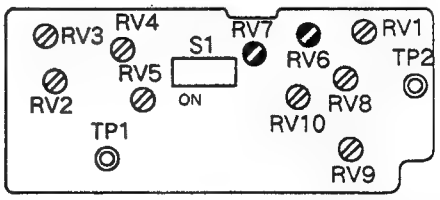

## ステップ7. VIDEOレベル調整（2）

注意事項
ステップ7. VIDEOレベル調整（2）からステップ8. SYNCレベル仮調整までの調整は連続して行って下さい。

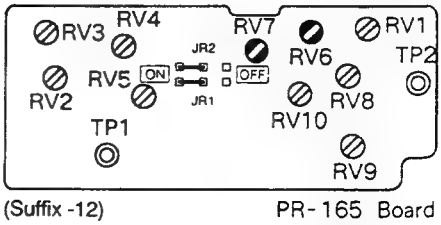
測定器： 波形モニター
被写体： グレースケールチャート
測定点： VIDEO OUT端子／リアパネル
調整箇所：◐RV6／PR-165基板
◐RV7／PR-165基板
準備： GAINスイッチ／リアパネル → M
※S1／PR-165基板（基板末尾-11） → ON
※JR1, JR2／PR-165基板（基板末尾-12） → ON
*基板末尾によって異なります。
規格： A＝100±2 IRE

調整手順
1. ◐RV6／PR-165基板にてA＝100±2 IREになるよう調整する。
2. S1／PR-165基板をOFFにする。
3. ◐RV7／PR-165基板にてA＝100±2 IREになるよう調整する。



(Suffix -11) PR-165 Board
－B Side－

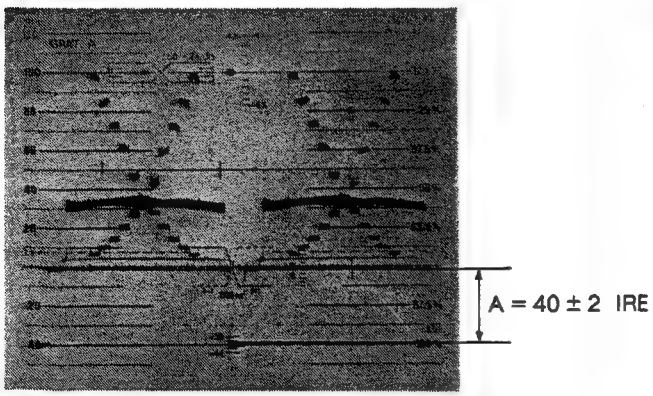


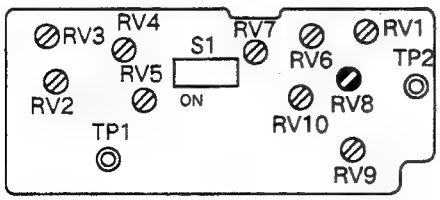
(Suffix -12) PR-165 Board
－B Side－

## ステップ8. SYNCレベル調整

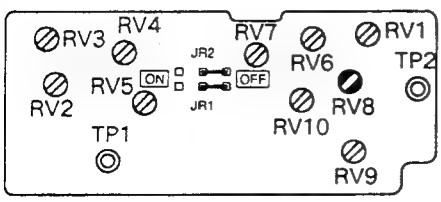
注意事項
この調整を行う前にステップ7. VIDEOレベル調整 (2) を済ませて下さい。

測定器： 波形モニター
被写体： グレースケールチャート
測定点： VIDEO OUT端子／リアパネル
調整箇所：●RV8／PR-165基板
準備： GAINスイッチ／リアパネル → M
※S1／PR-165基板 (基板末尾 -11) → OFF
※JR1, JR2／PR-165基板 (基板末尾 -12) → OFF
*基板末尾によって異なります。
規格： A = 40 ± 2 IRE
調整手順
1. 波形モニターにてVIDEO出力のSYNC部を確認する。
2. ●RV8／PR-165基板にてA = 40 ± 2 IREとなるように調整する。
3. この調整後、ステップ7. VIDEOレベル調整 (2) を再度行う。



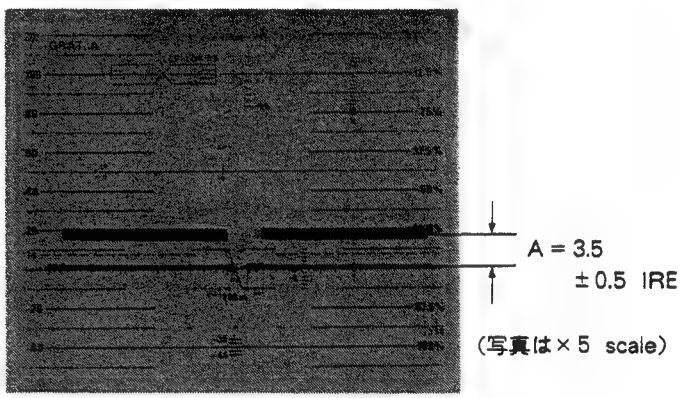
(Suffix -11) PR-165 Board – B Side –

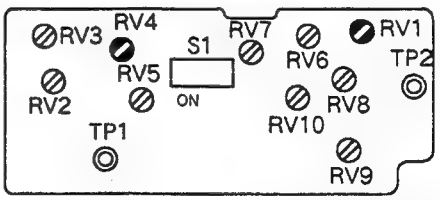


(Suffix -12) PR-165 Board – B Side –

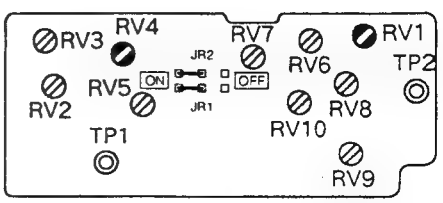
## ステップ9. PEDESTAL調整

測定器： 波形モニター
測定点： VIDEO OUT端子／リアパネル
調整箇所：●RV4／PR-165基板
●RV1／PR-165基板
準備： レンズ → クローズ
GAINスイッチ／リアパネル → F
※S1／PR-165基板 (基板末尾 -11) → ON
※JR1, JR2／PR-165基板 (基板末尾 -12) → ON
*基板末尾によって異なります。
規格： A = 3.5 ± 0.5 IRE
調整手順
(波形モニターのSCALE × 5にすると変化が読み取りやすくなります)
1. 波形モニターにてVIDEO出力を確認する。
2. ●RV4／PR-165基板にてA = 3.5 ± 0.5 IREとなるように調整する。
3. S1／PR-165基板をOFFにする。
4. ●RV1／PR-165基板にてA = 3.5 ± 0.5 IREとなるように調整する。



(Suffix -11) PR-165 Board – B Side –



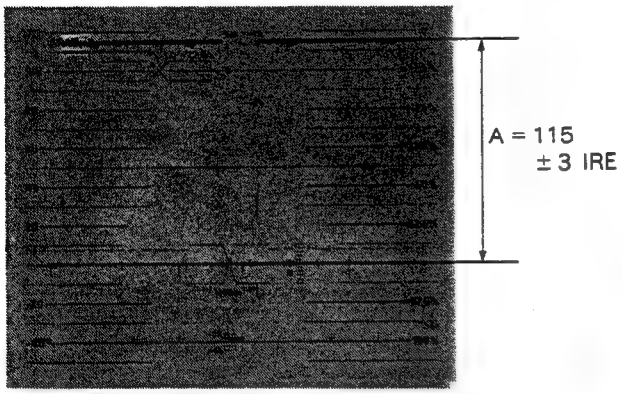
(Suffix -12) PR-165 Board – B Side –

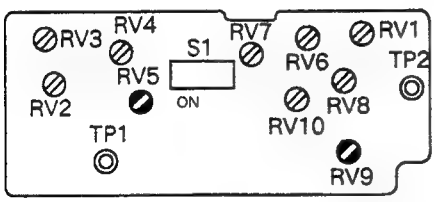
## ステップ10. WHITE CLIP調整

測定器： 波形モニター
測定点： VIDEO OUT端子／リアパネル
調整箇所：◐RV5／PR-165基板
準備： レンズ → 開放
GAINスイッチ／リアパネル → F
※S1／PR-165基板（基板末尾-11） → OFF
※JR1, JR2／PR-165基板（基板末尾-12） → OFF
*基板末尾によって異なります。
規格： A＝115±3 IRE

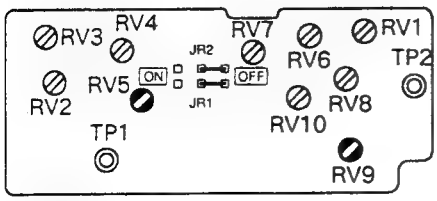
調整手順

1. 波形モニターにてVIDEO出力を確認する。
2. ◐RV5／PR-165基板にてA＝115±3 IREとなるように調整する。



(Suffix -11) PR-165 Board －B Side－



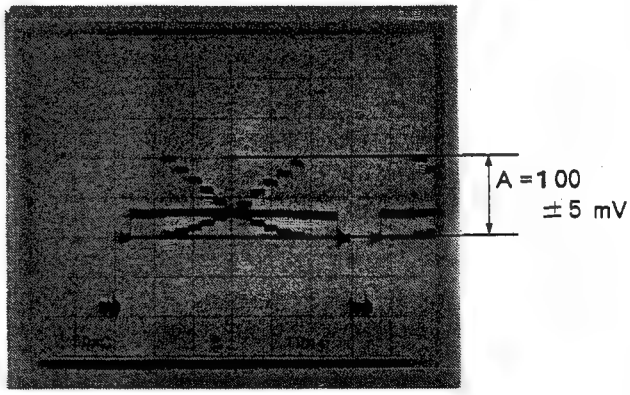
(Suffix -12) PR-165 Board －B Side－

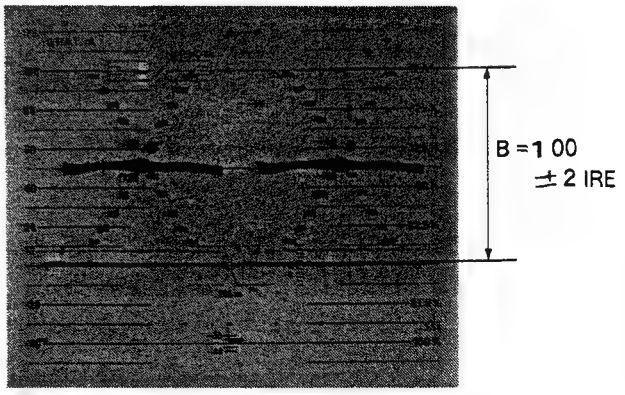
## ステップ11. AGC調整

測定器： オシロスコープ
波形モニター
被写体： グレースケールチャート（NDフィルター）
測定点： VIDEO OUT端子／リアパネル
調整箇所：◐RV9／PR-165基板
準備： GAINスイッチ／リアパネル → F
※S1／PR-165基板（基板末尾-11） → OFF
※JR1, JR2／PR-165基板（基板末尾-12） → OFF
*基板末尾によって異なります。
規格： A＝100±5 mV
B＝100±2 IRE

調整手順

1. レンズにNDフィルターを取り付ける。
2. グレースケールチャートを撮像しTP1／PR-165基板にて波形を確認する。
3. レンズ絞りにてA＝100±5 mVとなるよう調整する。
4. VIDEO出力を波形モニターにて確認する。
5. GAINスイッチ／リアパネルをAにする。
6. S1／PR-165基板をONにする。
7. ◐RV9／PR-165基板にてB＝100±2 IREとなるように調整する。



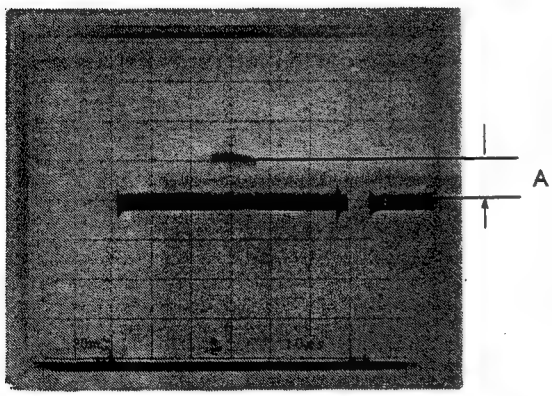
ステップ12. MAX GAIN調整

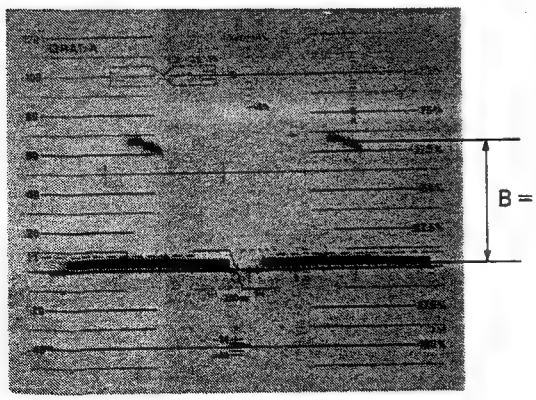
測定器： オシロスコープ
波形モニター
被写体： ウインドウチャート
測定点： VIDEO OUT端子／リアパネル
調整箇所：◐RV10／PR-165基板
準備： GAINスイッチ／リアパネル → A
※S1／PR-165基板 (基板末尾 -11) → OFF
※JR1, JR2／PR-165基板 (基板末尾 -12) → OFF
※基板末尾によって異なります。

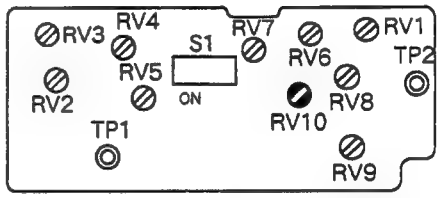
規格： B = 65 ± 2 IRE

調整手順

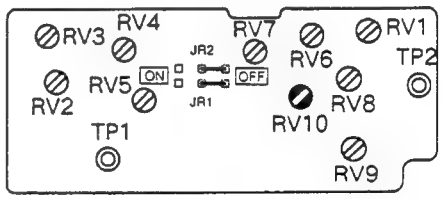
1. ウインドウチャートを撮像し、TP1／PR-165基板にて波形を確認する。
2. レンズ絞りにてA = 20 ± 1 mVとなるよう調整する。
3. VIDEO出力を波形モニターにて確認する。
4. ◐RV10／PR-165基板にてB = 65 ± 2 IREとなるように調整する。



(Suffix -11) PR-165 Board – B Side –



(Suffix -12) PR-165 Board – B Side –

調整終了後：

- PR-165基板のJR1とJR2 (基板末尾が -11 の場合は、S1) は、ユーザー側の要求に合わせてON、またはOFFに設定します。

- 下記のスイッチを設定して下さい。
  S2／SG-199基板 → ON
  S3／SG-199基板 → ON
  ゲインスイッチ／リアパネル → F

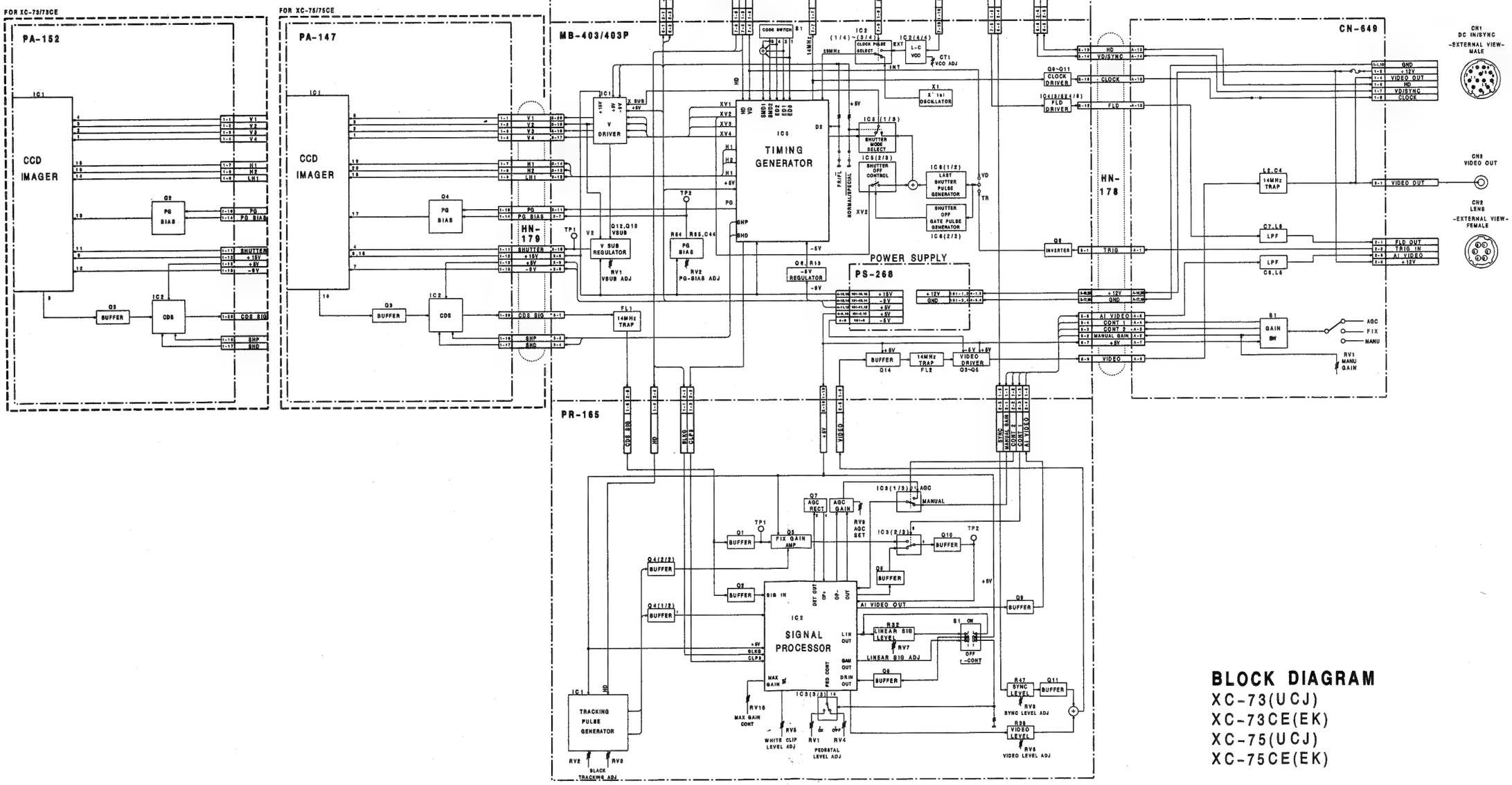
# 目 次

B. SEMICONDUCTOR

C. SPARE PARTS

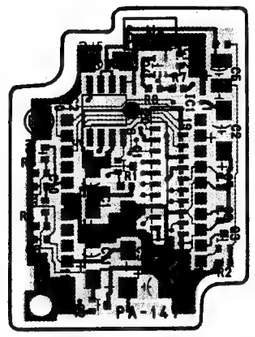
# SECTION A DIAGRAM

## BLOCK DIAGRAM

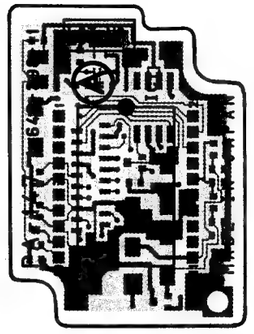



**BLOCK DIAGRAM**
XC-73(UCJ)
XC-73CE(EK)
XC-75(UCJ)
XC-75CE(EK)

## PA-147 BOARD(XC-75/75CE)

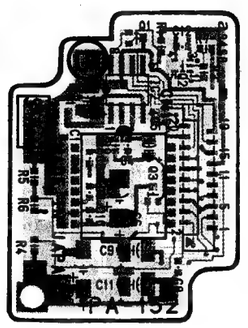


-COMPONENT SIDE-
1-642-398-11

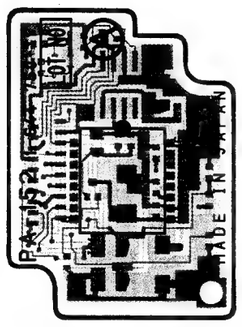


-SOLDERING SIDE-
1-642-398-11

## PA-152 BOARD(XC-73/73CE)

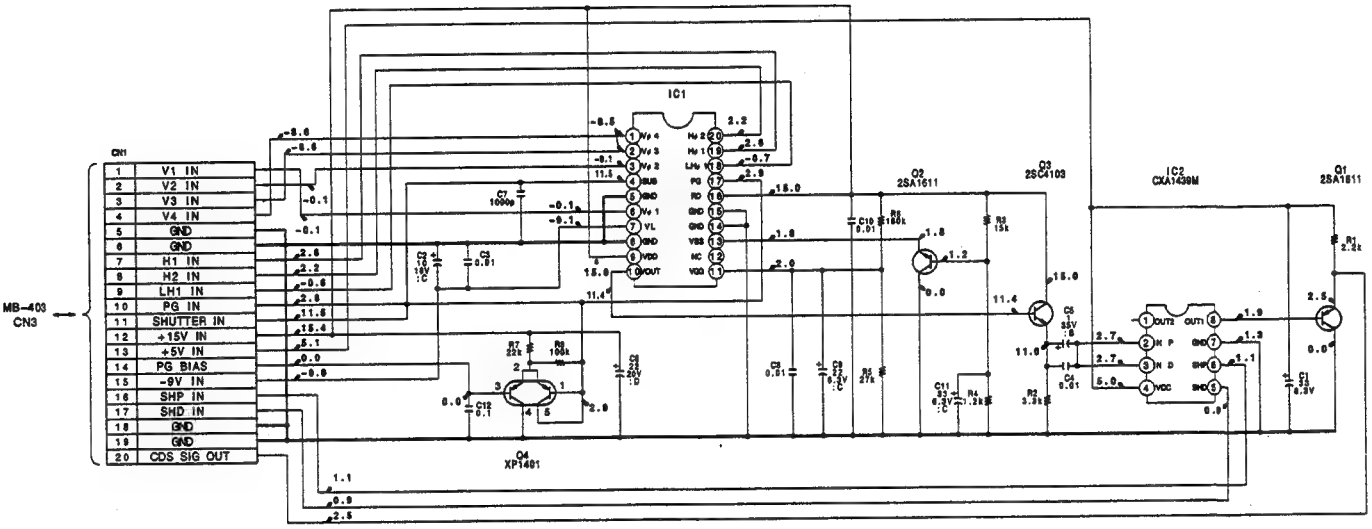


-COMPONENT SIDE-
1-644-750-11



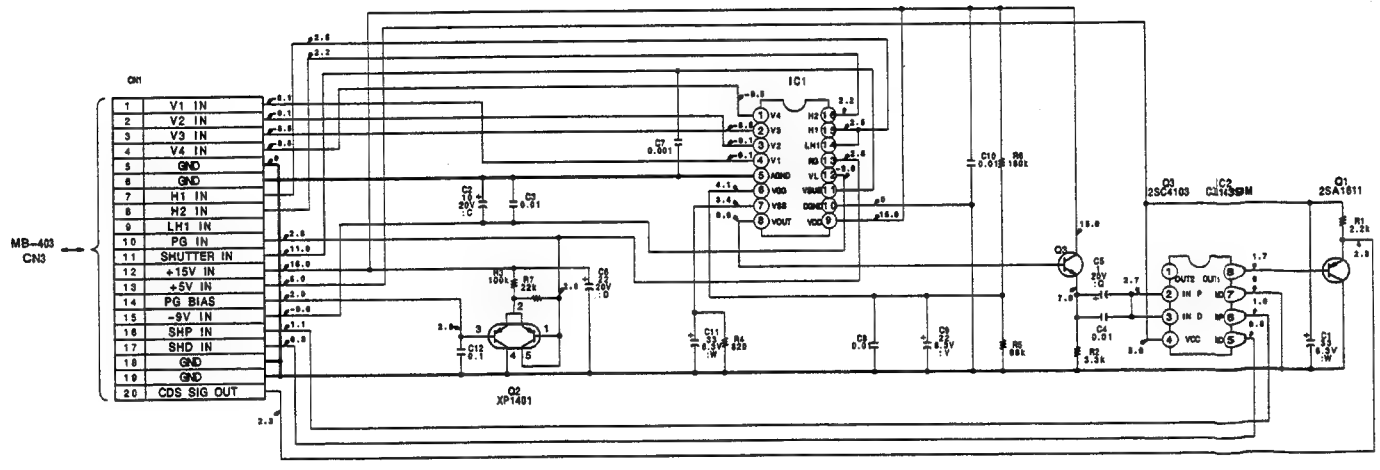
-SOLDERING SIDE-
1-644-750-11

## PA-147 BOARD(XC-75/75CE)




**PA-147 BOARD**
XC-75(UCJ)
XC-75CE(EK)

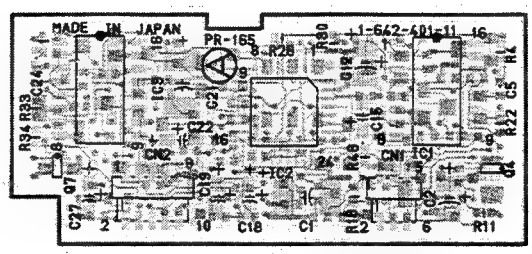
## PA-152 BOARD(XC-73/73CE)




**PA-152 BOARD**
XC-73(UCJ)
XC-73CE(EK)

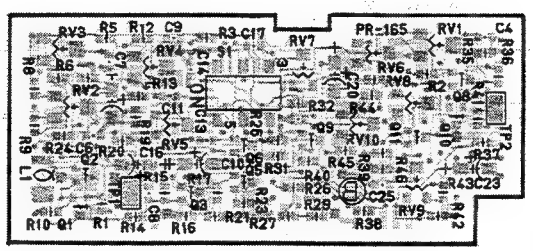
## PR-165 BOARD

| | | | |
|---|---|---|---|
| Serial | No.10001 | to 60900 | (XC-75) |
| Serial | No.10001 | to 53000 | (XC-75CE) |
| Serial | No.10001 | to 15550 | (XC-73) |
| Serial | No.400001 | to 405150 | (XC-73CE) |




-COMPONENT SIDE-

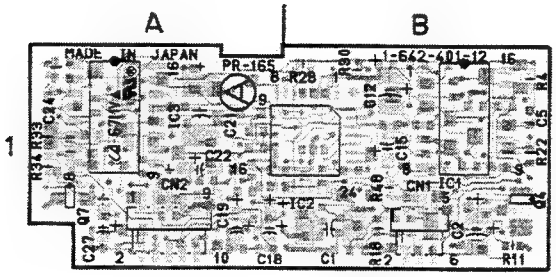
1-642-401-11




-SOLDERING SIDE-

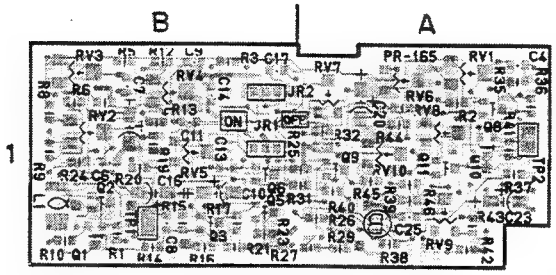
1-642-401-11

| | | | |
|---|---|---|---|
| Serial | No.60901 | and higher | (XC-75) |
| Serial | No.53001 | and higher | (XC-75CE) |
| Serial | No.15551 | and higher | (XC-73) |
| Serial | No.405151 | and higher | (XC-73CE) |




-COMPONENT SIDE-

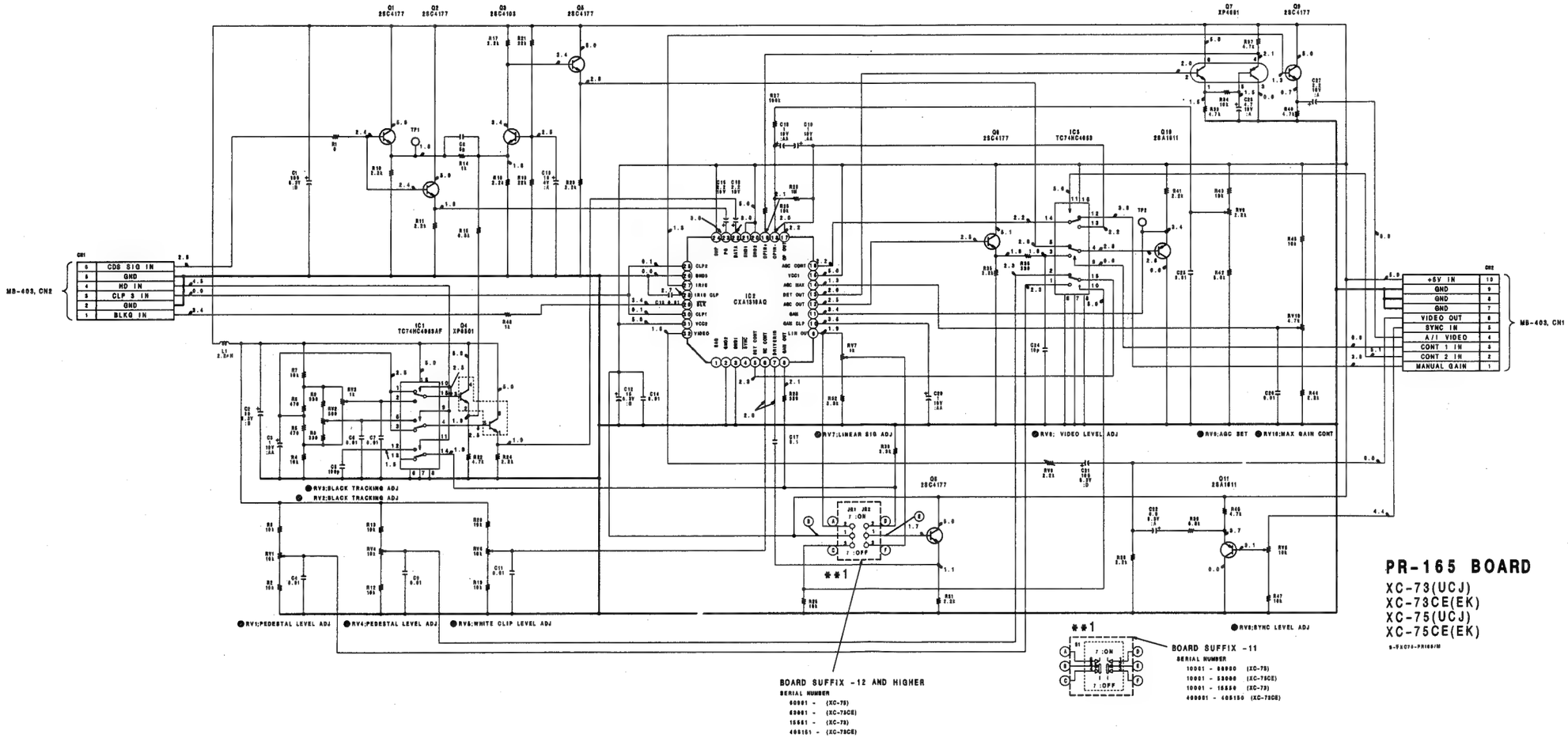
1-642-401-12




-SOLDERING SIDE-

1-642-401-12

## PR-165 BOARD




**PR-165 BOARD**
XC-73(UCJ)
XC-73CE(EK)
XC-75(UCJ)
XC-75CE(EK)
B-¥XC75-PR165/M

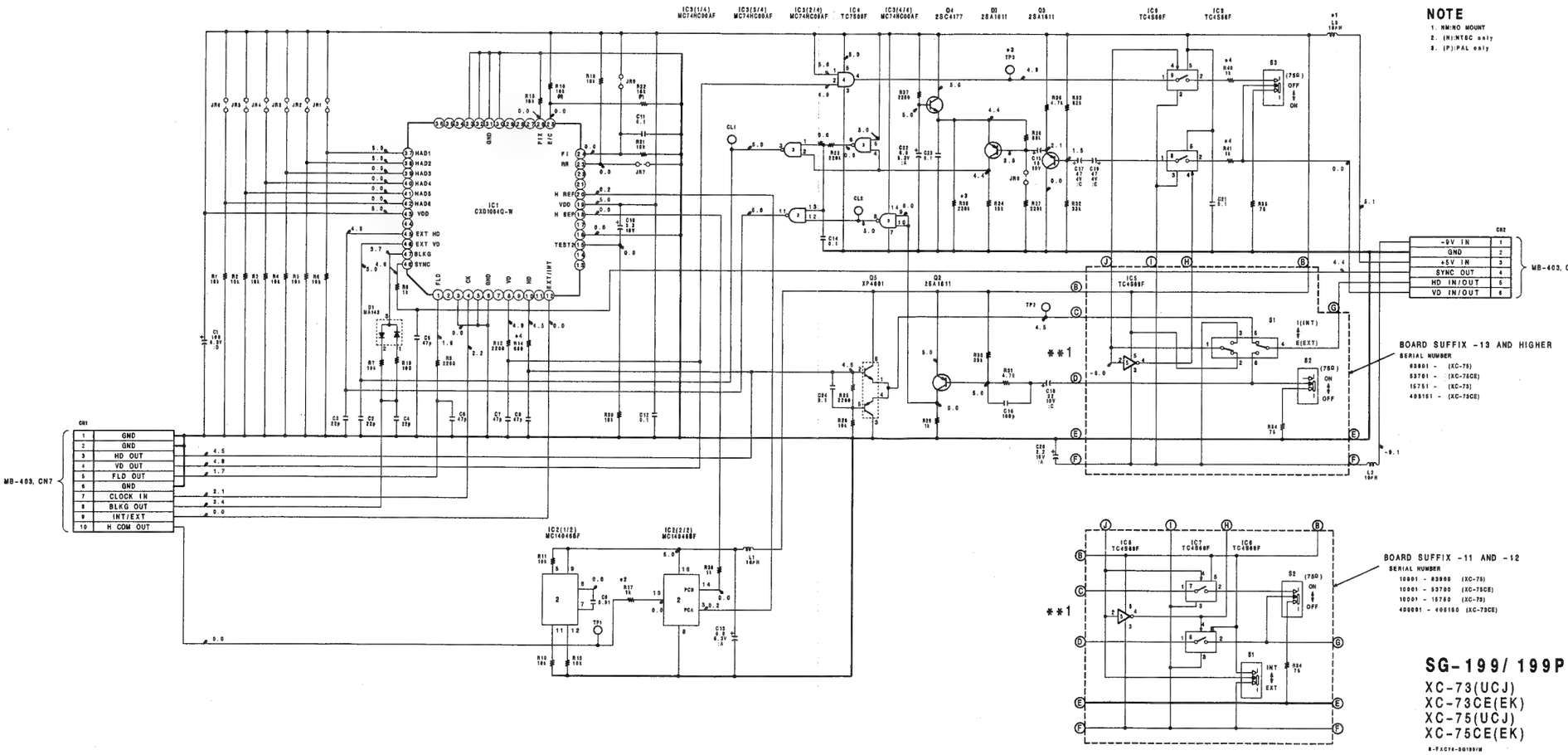
## SG-199/199P BOARD

CHANGE INFORMATION

| MARK | REF. NO. | CHANGE INFORMATION | SERIAL NO. |
|---|---|---|---|
| ※1 | L3 | 47uH → 10mH | 11601 -(XC-75)<br>10601 -(XC-75CE)<br>10301 -(XC-73)<br>400001 -(XC-73CE) |
| ※2 | R17 | 10K → 1K | 31801 -(XC-75)<br>17701 -(XC-75CE)<br>11271 -(XC-73)<br>400301 -(XC-73CE) |
| ※3 | R39 | ADD 220K | 11001 - (XC-75)<br>10401 - (XC-75CE) |
| | TP3 | DELETE TP3 | 10001 - (XC-73)<br>400001 - (XC-73CE) |

CHANGE INFORMATION

| MARK | REF. NO. | CHANGE INFORMATION | SERIAL NO. |
|---|---|---|---|
| ※4 | R40 | ADD 1K | 63901 - (XC-75)<br>53751 - (XC-75CE) |
| | R41 | | 15751 - (XC-73)<br>405151 - (XC-73CE) |
| | R14 | 220 → 680 | |




**NOTE**
1. NM:NO MOUNT
2. (N):NTSC only
3. (P):PAL only

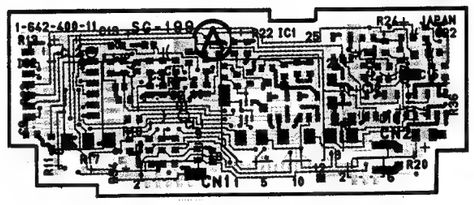
**SG-199/ 199P BOARD**

XC-73(UCJ)
XC-73CE(EK)
XC-75(UCJ)
XC-75CE(EK)

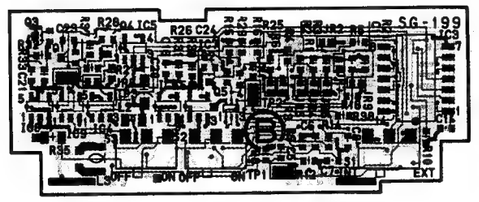
B-FXC74-SG199/M

## SG-199/199P BOARD

Serial No.10001 to 11000 (XC-75)
Serial No.10001 to 10400 (XC-75CE)

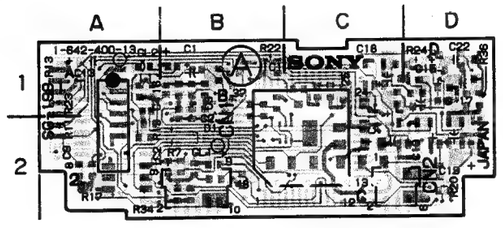


-COMPONENT SIDE-
1-642-400-11

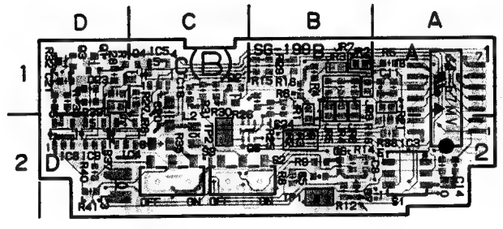


-SOLDERING SIDE-
1-642-400-11

Serial No.63901 and higher (XC-75)
Serial No.53701 and higher (XC-75CE)
Serial No.15751 and higher (XC-73)
Serial No.405151 and higher (XC-73CE)

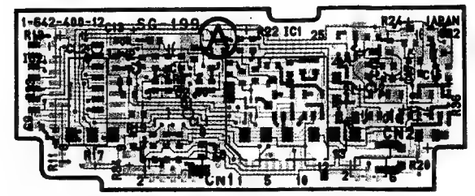


-COMPONENT SIDE-
1-642-400-13

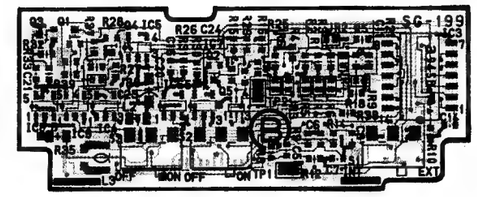


-SOLDERING SIDE-
1-642-400-13

Serial No.11001 to 63900 (XC-75)
Serial No.10401 to 53700 (XC-75CE)
Serial No.10001 to 15750 (XC-73)
Serial No.400001 to 405150 (XC-73CE)



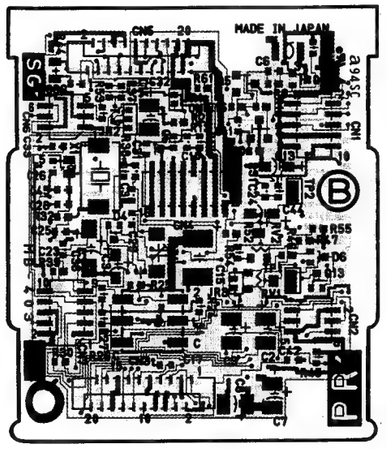
-COMPONENT SIDE-
1-642-400-12



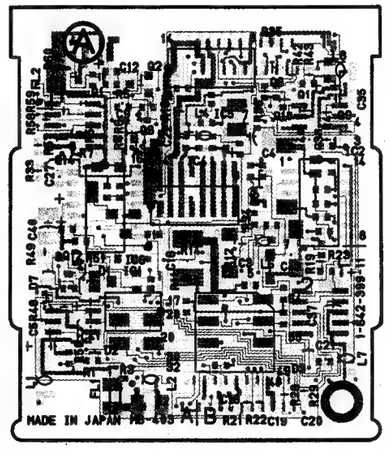
-SOLDERING SIDE-
1-642-400-12

## MB-403/403P BOARD

Serial No.10001 to 10600 (XC-75)
Serial No.10001 to 10200 (XC-75CE)

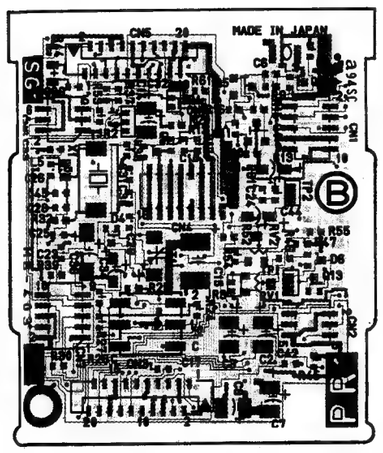


-COMPONENT SIDE-
1-642-399-11

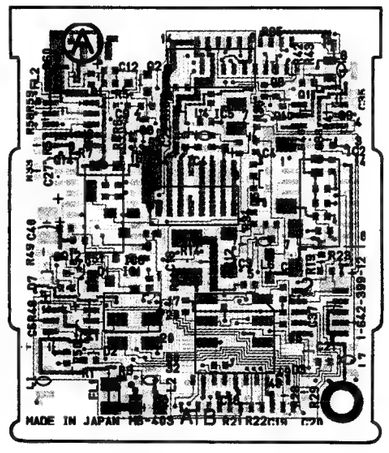


-SOLDERING SIDE-
1-642-399-11

Serial No.10601 and higher (XC-75)
Serial No.10201 and higher (XC-75CE)
Serial No.10001 and higher (XC-73)
Serial No.400001 and higher (XC-73CE)



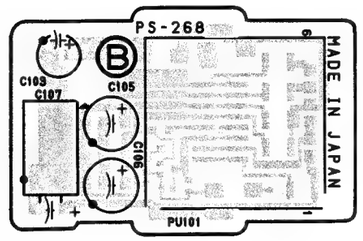
-COMPONENT SIDE-
1-642-399-12



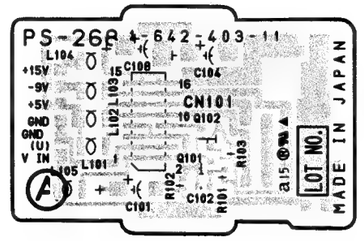
-SOLDERING SIDE-
1-642-399-12

## PS-268 BOARD

Serial No.10001 to 10300 (XC-75)
Serial No.10001 to 10100 (XC-75CE)

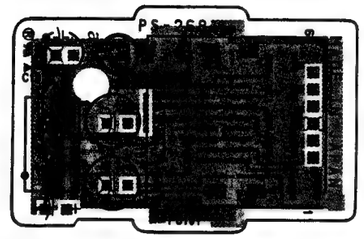



-COMPONENT SIDE-
1-642-403-11

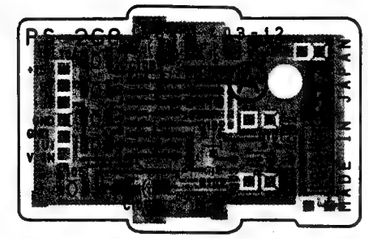



-SOLDERING SIDE-
1-642-403-11

Serial No.10301 and higher (XC-75)
Serial No.10101 and higher (XC-75CE)
Serial No.10001 and higher (XC-73)
Serial No.400001 and higher (XC-73CE)

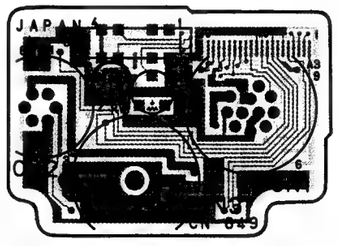


-COMPONENT SIDE-
1-642-403-12

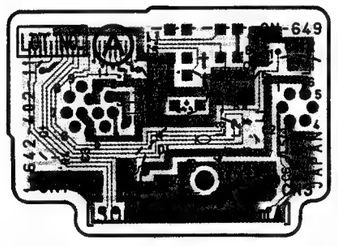


-SOLDERING SIDE-
1-642-403-12

## CN-649 BOARD



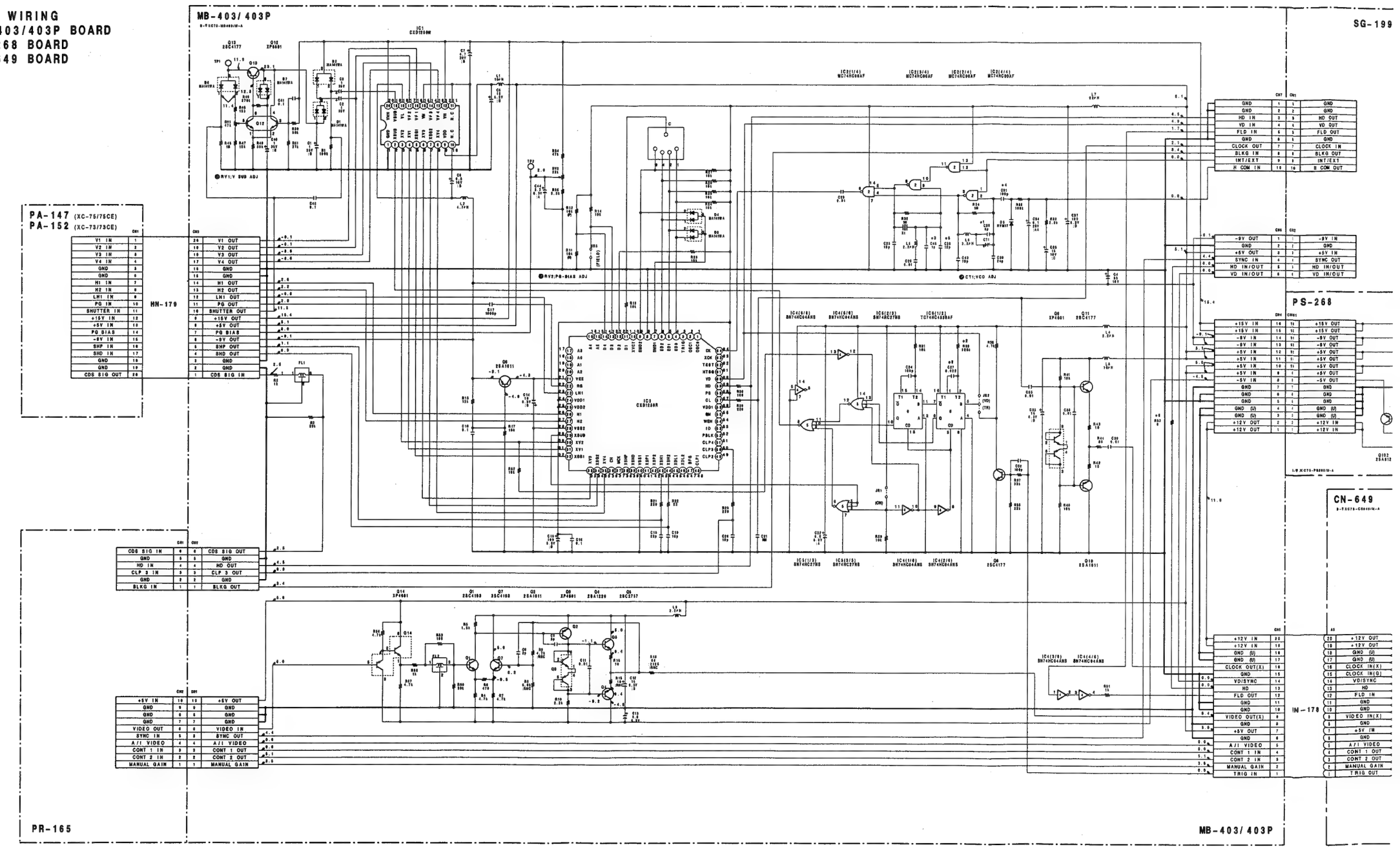
-COMPONENT SIDE-
1-642-402-11



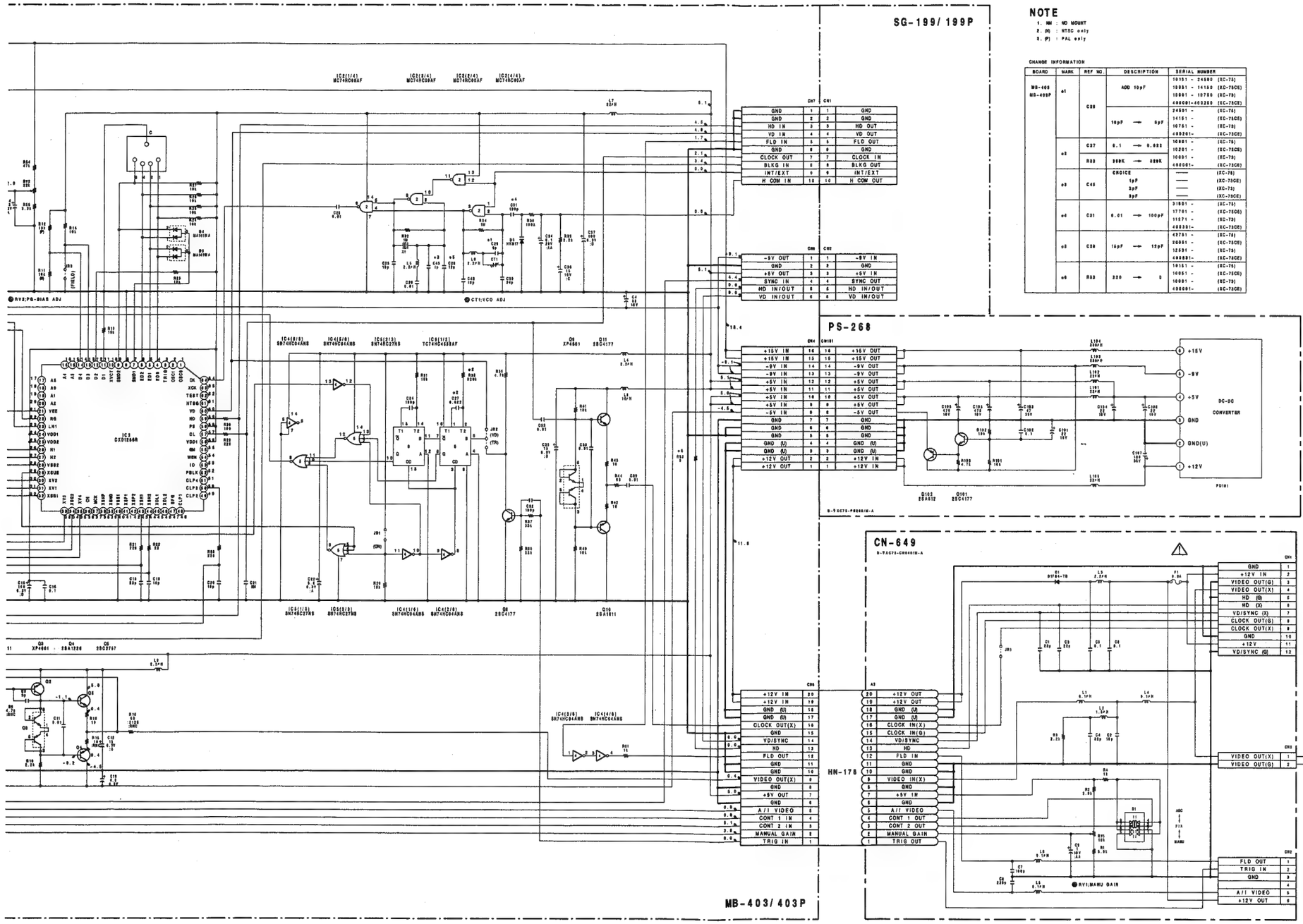
-SOLDERING SIDE-
1-642-402-11

FRAME MB-403/403P, PS-268, CN-649

## FRAME WIRING
MB-403/403P BOARD
PS-268 BOARD
CN-649 BOARD




XC-75(UCJ)
XC-75CE(EK)
A-¥XC75-FRAME/M




NOTE

1. NM : NO MOUNT
2. (N) : NTSC only
3. (P) : PAL only

CHANGE INFORMATION

| BOARD | MARK | REF NO. | DESCRIPTION | SERIAL NUMBER |
|---|---|---|---|---|
| MB-405 MB-403P | a1 | C28 | ADD 10pF | 10151 - 24599 (XC-75) |
| | | | | 19351 - 14159 (XC-75CE) |
| | | | | 13661 - 10759 (XC-73) |
| | | | | 400501-403209 (XC-73CE) |
| | | | 10pF → 8pF | 24591 - (XC-75) |
| | | | | 14151 - (XC-75CE) |
| | | | | 10751 - (XC-73) |
| | | | | 403201- (XC-73CE) |
| | a2 | C27 | 0.1 → 0.022 | 10601 - (XC-75) |
| | | | | 10201 - (XC-75CE) |
| | | R23 | 220K → 220K | 10001 - (XC-73) |
| | | | | 400001- (XC-73CE) |
| | a3 | C45 | CHOICE | —— (XC-75) |
| | | | 1pF | —— (XC-75CE) |
| | | | 2pF | —— (XC-73) |
| | | | 3pF | —— (XC-73CE) |
| | a4 | C21 | 0.01 → 100pF | 31801 - (XC-75) |
| | | | | 17701 - (XC-75CE) |
| | | | | 11271 - (XC-73) |
| | | | | 402301- (XC-73CE) |
| | a5 | C26 | 15pF → 12pF | 43751 - (XC-75) |
| | | | | 26051 - (XC-75CE) |
| | | | | 12531 - (XC-73) |
| | | | | 402891- (XC-73CE) |
| | a6 | R22 | 220 → 0 | 19151 - (XC-75) |
| | | | | 16051 - (XC-75CE) |
| | | | | 16001 - (XC-73) |
| | | | | 400891- (XC-73CE) |

## FRAME WIRING

MB-403/403P BOARD
PS-268 BOARD
CN-649 BOARD
XC-75(UCJ)
XC-75CE(EK)
XC-73(UCJ)
XC-73CE(EK)

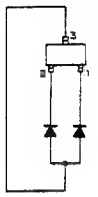
A-▼XC75-FRAME/M
B-▼XC75-MB403/M-A
B-▼XC75-CN649/M-A
B-▼XC75-PS268/M-A

# SECTION B
# SEMICONDUCTOR

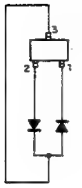
The circuit diagram of IC is obtaind from the IC data book published by the manufacture.

## <Diode>

1SS181

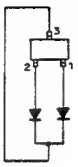


1SS226

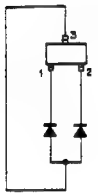


D1FS4

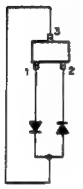
HVM17-01



MA141WA

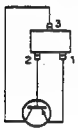


MA143

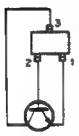


## <Transistor>

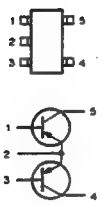
2SA1162
2SA1226
2SA1611
2SA812



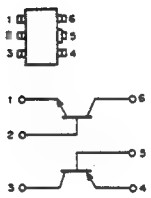
2SC2757
2SC4103
2SC4177



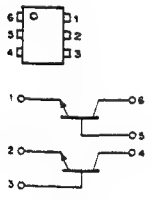
XP1401



XP4601

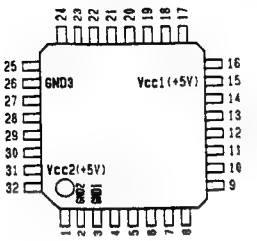


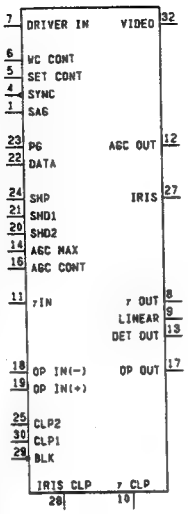
XP6501



CXA1310AQ (SONY)

1-CHIP PROCESS FOR CCD BLACK AND WHITE
– TOP VIEW –

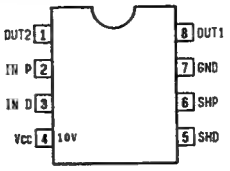


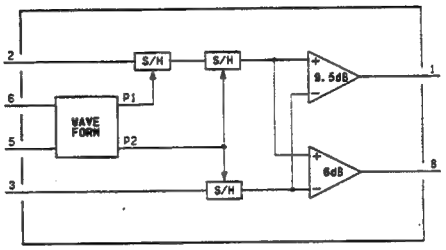




| PIN No. | I/O | SIGNAL | PIN No. | I/O | SIGNAL |
|---|---|---|---|---|---|
| 1 | I | SAG | 17 | O | OP OUT |
| 2 | – | GND2 | 18 | I | OP IN (–) |
| 3 | – | GND1 | 19 | I | OP IN (+) |
| 4 | I | SYNC | 20 | I | SHD2 |
| 5 | I | SET CONT | 21 | I | SHD1 |
| 6 | I | WC CONT | 22 | I | DATA |
| 7 | I | DRIVER IN | 23 | I | PG |
| 8 | O | γ OUT | 24 | I | SHP |
| 9 | O | LINEAR | 25 | I | CLP2 |
| 10 | I | γ CLP | 26 | – | GND3 |
| 11 | I | γ IN | 27 | O | IRIS |
| 12 | O | AGC OUT | 28 | I | IRIS CLP |
| 13 | O | DET OUT | 29 | I | BLK |
| 14 | I | AGC MAX | 30 | I | CLP1 |
| 15 | – | Vcc1 | 31 | – | Vcc2 |
| 16 | I | AGC CONT | 32 | O | VIDEO |

CXA1439M (SONY) FLAT PACKAGE

CORRELATED DOUBLE SAMPLING
– TOP VIEW –



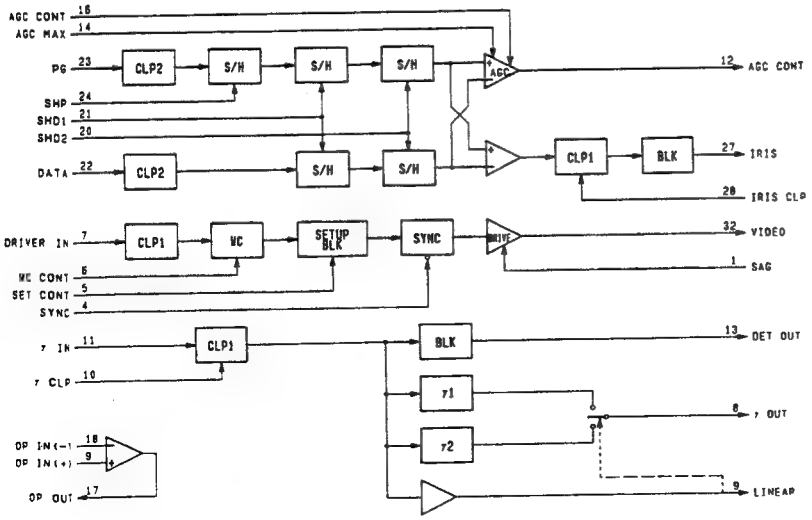




**INPUT**

AGC CONT : AGC AMPLIFIER GAIN CONTROL
AGC MAX : AGC AMPLIFIER MAX GAIN
BLK : BLK PULSE INPUT
CLP1, 2 : CLP1, 2 PULSE INPUT
DATA : CCD SIGNAL INPUT
DRIVER IN : DRIVER INPUT
IRIS CLP : IRIS OUTPUT CLAMP
OP IN (+) : OPERATIONAL AMPLIFIER NON-TURX INPUT
OP IN (–) : OPERATIONAL AMPLIFIER TURN INPUT
PG : CCD SIGNAL INPUT
SAG : SAG CORRECTION SIGNAL INPUT
SET CONT : SETUP LEVEL ADJUSTMENT
SHD1, 2 : SAMPLE HOLD PULSE INPUT
SHP : SAMPLE HOLD PULSE INPUT
SYNC : SYNC PULSE INPUT
WC CONT : WHITE CLIP LEVEL ADJUSTMENT
γ CLP : γ INPUT CLAMP
γ IN : γ ADJUSTMENT INPUT

**OUTPUT**

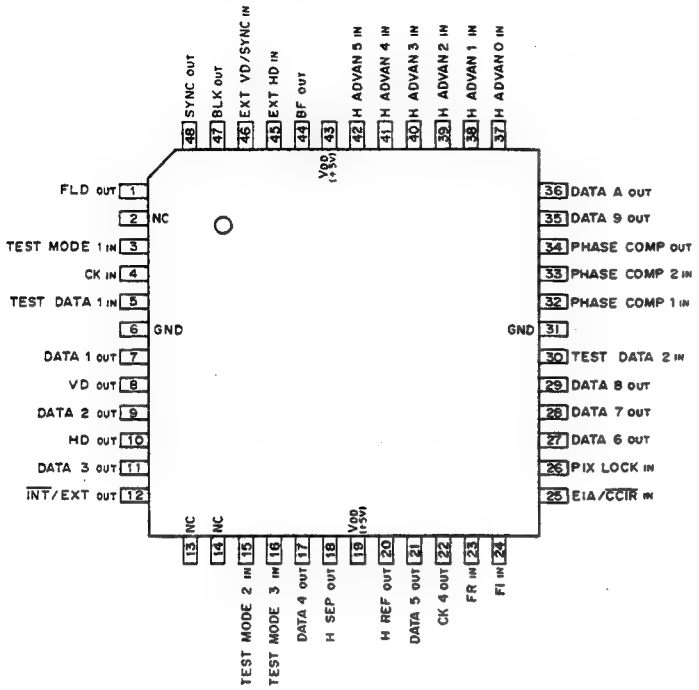
AGC OUT : AGC SIGNAL OUTPUT
DET OUT : AGC DETECTION SIGNAL OUTPUT
IRIS : IRIS CONTROL SIGNAL OUTPUT
LINEAR : LINEAR SIGNAL OUTPUT
OP OUT : OPERATIONAL AMPLIFIER OUTPUT
VIDEO : VIDEO SIGNAL OUTPUT
γ OUT : γ CORRECTION SIGNAL OUTPUT

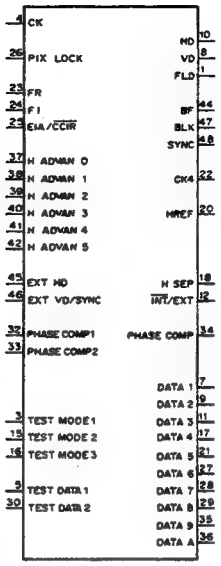


CXD1084Q-W (SONY) FLAT PACKAGE

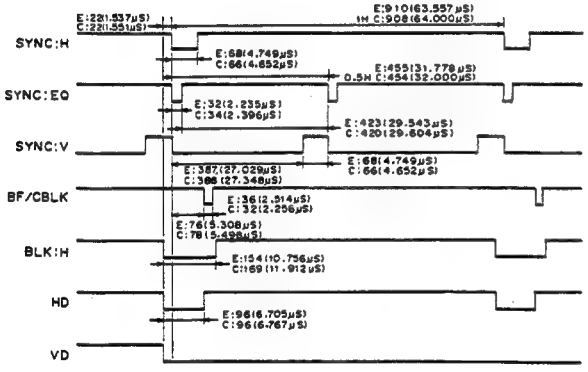
C-MOS SYNC GENERATOR FOR CCD B/W CAMERA

– TOP VIEW –



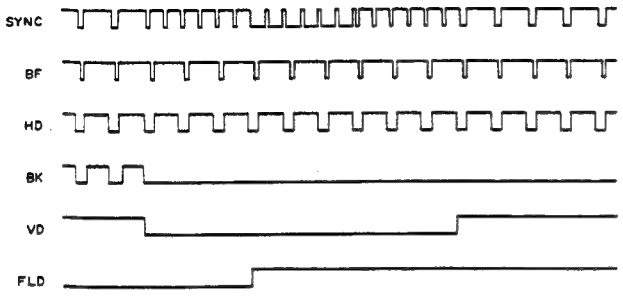

CK ; EIA = 910FH CCIR = 908FH
PIX LOCK ; PIXEL LOCK MODE SELECT
FR ; FIELD RESET MODE SELECT
FI ; FIELD INVERSION MODE SELECT
EXT HD ; EXTERNAL HD
EXT VD/SYNC ; EXTERNAL VD or SYNC
H ADVAN 0~5 ; H REF PULSE DELAY CONTROL DATA
CK4 ; QUARTER CK PULSE



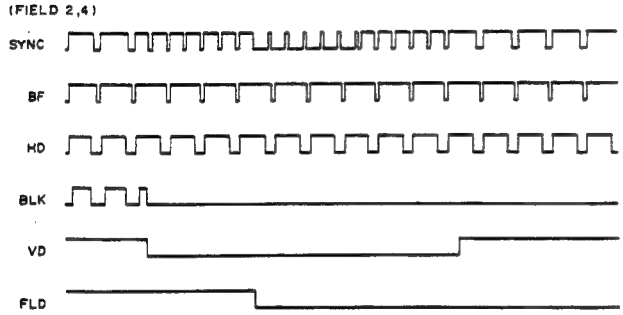

E ; EIA
C ; CCIR

※ Values in parenthesis ( ) are on the basis of the following clocks.
EIA CK : 14.31818MHz
CCIR CK : 14.1875MHz

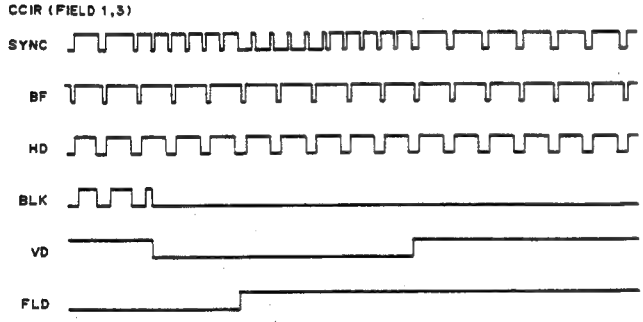
EIA (FIELD 1,3)



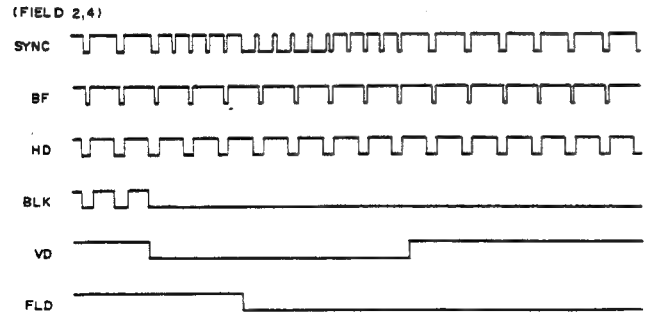

(FIELD 2,4)




CCIR (FIELD 1,3)



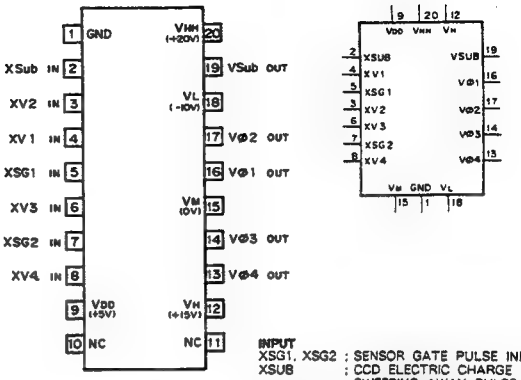

(FIELD 2,4)




CXD1250N (SONY) FLAT PACKAGE

C-MOS VERTICAL CLOCK DRIVER FOR CCD

– TOP VIEW –




**INPUT**

XSG1, XSG2 : SENSOR GATE PULSE INPUT

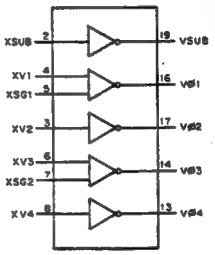
XSUB : CCD ELECTRIC CHARGE SWEEPING AWAY PULSE INPUT

XV1-XV4 : VERTICAL REGISTER TRANSMISSION CLOCK INPUT

**OUTPUT**

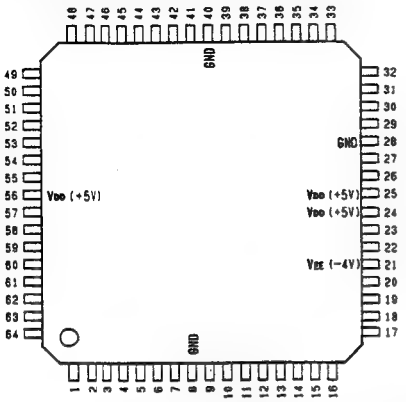
VSUB : CCD ELECTRIC CHARGE SWEEPING AWAY PULSE OUTPUT

V ϕ 1-V ϕ 4 : VERTICAL REGISTER TRANSMISSION CLOCK OUTPUT



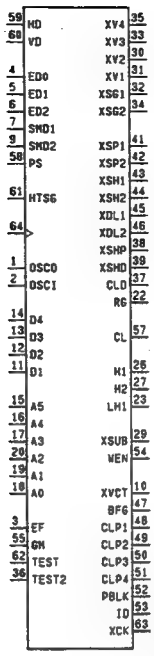
CXD1256AR (SONY) FLAT PACKAGE

TIMING GENERATOR FOR CCD CAMERA
– TOP VIEW –




(VDD=+5V)
(VEE=–4V)

| Pin No. | I/O | SYMBOL | Pin No. | I/O | SYMBOL | Pin No. | I/O | SYMBOL | Pin No. | I/O | SYMBOL |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | O | OSCO | 17 | O | A3 | 33 | O | XV3 | 49 | I/O | CLP2 |
| 2 | I | OSCI | 18 | O | A0 | 34 | O | XSG2 | 50 | I/O | CLP3 |
| 3 | I | EF | 19 | O | A1 | 35 | O | XV4 | 51 | O | CLP4 |
| 4 | I | ED0 | 20 | O | A2 | 36 | I | TEST2 | 52 | O | PBLK |
| 5 | I | ED1 | 21 | – | VEE | 37 | O | CLD | 53 | O | ID |
| 6 | I | ED2 | 22 | O | RG | 38 | O | XSHP | 54 | O | WEN |
| 7 | I | SMD1 | 23 | – | LH1 | 39 | O | XSHD | 55 | I | GM |
| 8 | – | GND | 24 | – | VDD | 40 | – | GND | 56 | – | VDD |
| 9 | I | SMD2 | 25 | – | VDD | 41 | O | XSP1 | 57 | O | CL |
| 10 | O | XVCT | 26 | O | H1 | 42 | O | XSP2 | 58 | I | PS |
| 11 | I | D1 | 27 | O | H2 | 43 | O | XSH1 | 59 | I | HD |
| 12 | I | D2 | 28 | – | GND | 44 | O | XSH2 | 60 | I | VD |
| 13 | I | D3 | 29 | O | XSUB | 45 | O | XDL1 | 61 | I | HTSG |
| 14 | I | D4 | 30 | O | XV2 | 46 | O | XDL2 | 62 | I | TEST |
| 15 | O | A5 | 31 | O | XV1 | 47 | O | BFG | 63 | O | XCK |
| 16 | O | A4 | 32 | O | XSG1 | 48 | O | CLP1 | 64 | I | CK |




**INPUT**

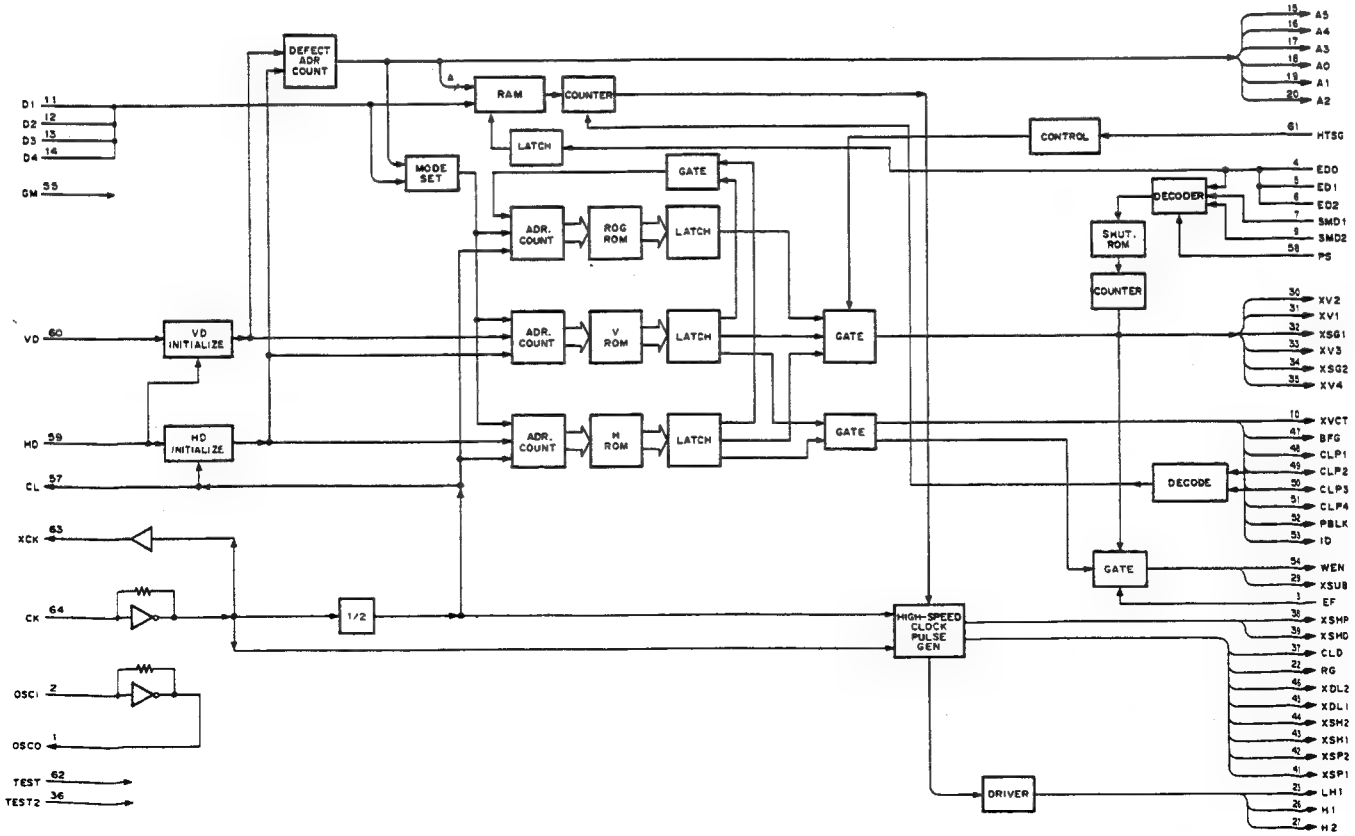
| | |
|---|---|
| CK | : 8fsc CLOCK |
| D1 | : WHEN EXTERNAL ROM IS USED, DATA INPUT. WHEN NOT USED, L : NO ERROR COMPENSATION |
| D2 | : WHEN EXTERNAL ROM IS USED, DATA INPUT WHEN NOT USED, L : COLOR H : B/W |
| D3 | : WHEN EXTERNAL ROM IS USED, DATA INPUT. WHEN NOT USED, FIXED TO LOW |
| D4 | : WHEN EXTERNAL ROM IS USED, DATA INPUT. WHEN NOT USED, L : NTSC H : PAL |
| ED0 | : SHUTTER SPEED SET. WHEN SERIAL MODE, STROBE INPUT. |
| ED1 | : SHUTTER SPEED SET. WHEN SERIAL MODE, CLOCK INPUT. |
| ED2 | : SHUTTER SPEED SET. WHEN SERIAL MODE, DATA INPUT. |
| EF | : DATA INPUT METHOD CHANGE FOR ERROR COMPENSATION<br>H : EXTERNAL ROM USED<br>L : SERIAL INPUT FROM MICROPROCESSOR |
| GM | : L : FOR ANALOG SIGNAL, H : FOR DIGITAL SIGNAL |
| HD | : HORIZONTAL DRIVE |
| HTSG | : XSG1, XSG2 CONTROL<br>H : XSG1 AND 2 GENERATED<br>L : XSG1 AND 2 STOPPED |
| OSCI | : INVERTER INPUT FOR OSCILLATION |
| PS | : ELECTRONIC SHUTTER SPEED INPUT METHOD CHANGE<br>H : PARALLEL INPUT<br>L : SERIAL INPUT |
| SMD1, SMD2 | : SHUTTER MODE SET |
| TEST, TEST2 | : FOR TEST (NORMALLY Low) |
| VD | : VERTICAL DRIVE |

**OUTPUT**

| | |
|---|---|
| AS-A0 | : ADDRESS FOR EXTERNAL ROM |
| BFG | : PULSE FOR ENCODER • CHROMA MODULATOR WHEN GM = H, ERROR POSITION SPECIFING PULSE |
| CL | : 4fsc CLOCK |
| CLD | : 4fsc CLOCK |
| CLP1, CLP4 | : PULSE FOR CLAMP |
| H1, H2 | : CLOCK FOR CCD HORIZONTAL REGISTER DRIVE |
| ID | : LINE IDENTIFICATION |
| OSCO | : INVERTER OUTPUT FOR OSCILLATION |
| PBLK | : BLANKING CLEANING PULSE |
| RG | : RESET GATE PULSE |
| WEN | : WRITE ENABLE (ONLY WHEN LOW SHUTTER SPEED) |
| XCK | : 8fsc CLOCK |
| XDL1, XDL2 | : CLOCK FOR DELAY LINE |
| XSG1, XSG2 | : CCD SENSOR ELECTRIC CHARGE READ OUT PULSE |
| XSH1, XSH2 | : SWITCHING SAMPLE HOLD PULSE |
| XSHD | : PULSE FOR DATA SAMPLE HOLD |
| XSHP | : PRE-CHARGE LEVEL SAMPLE HOLD PULSE |
| XSP1, XSP2 | : CHROMA SEPARATION SAMPLE HOLD PULSE |
| XSUB | : ELECTRIC CHARGE DISCHARGING PULSE |
| XV1-XV4 | : VERTICAL SCANNING CLOCK |
| XVCT | : POWER CONTROL FOR EXTERNAL ROM |

**INPUT/OUTPUT**

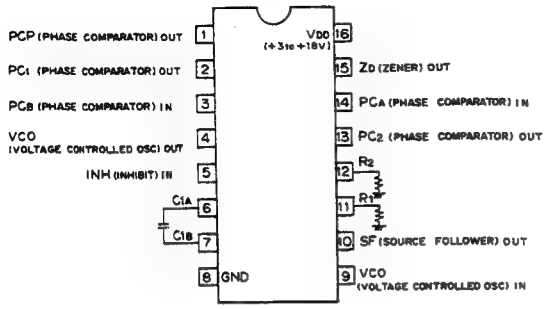
| | |
|---|---|
| CLP2, CLP3 | : PULSE FOR CLAMP. WHEN GM = H, STANDBY MODE SWITCHING INPUT |

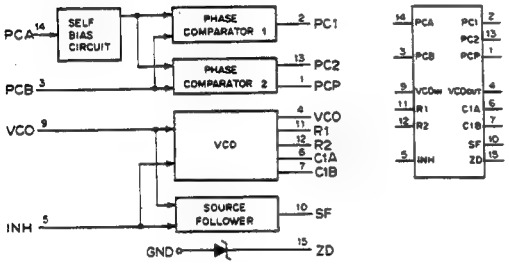


MC14046BF (MOTOROLA) FLAT PACKAGE

C-MOS PHASE LOCKED LOOP

– TOP VIEW –

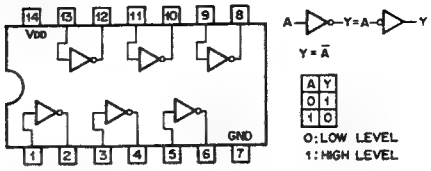



SN74HC04ANS (TI) FLAT PACKAGE

C-MOS HEX INVERTERS

– TOP VIEW –



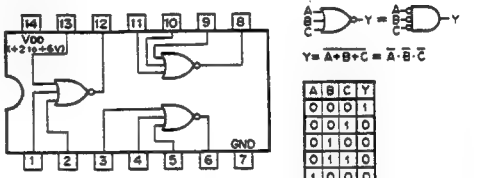

NOTE :

| TYPE | VDD |
|---|---|
| 74HCT04 TYPE | +5V |
| TC74AC04 TYPE | +2 to +5.5V |
| 74ACT04 TYPE | +4.5 to +5.5V |
| OTHER TYPES | +2 to +6V |

SN74HC27ANS (TI) FLAT PACKAGE

C-MOS 3-LINE POSITIVE-NOR GATE

– TOP VIEW –



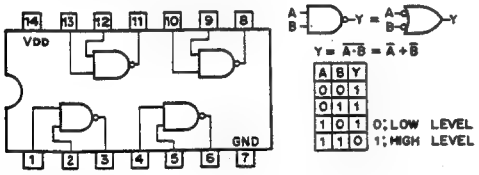

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

0 ; LOW LEVEL
1 ; HIGH LEVEL

MC74HC00AF (MOTOROLA) FLAT PACKAGE
SN74HC00ANS (TI) FLAT PACKAGE

C-MOS QUAD 2-INPUT NAND GATES

– TOP VIEW –




| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

0 ; LOW LEVEL
1 ; HIGH LEVEL

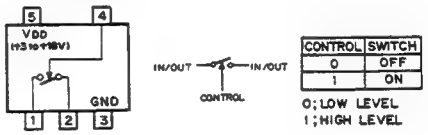
NOTE :

| TYPE | VDD |
|---|---|
| TC74AC00 TYPE | +2 to +5.5V |
| MC74HCT00N | +5V |
| 74ACT00 TYPE | +4.5 to +5.5V |
| OTHER TYPES | +2 to +6V |

TC4S66F (TOSHIBA)

C-MOS BILATERAL ANALOG SWITCH

– TOP VIEW –



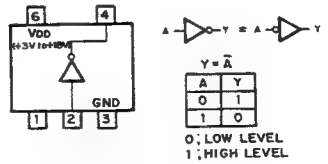

| CONTROL | SWITCH |
|---|---|
| 0 | OFF |
| 1 | ON |

0 ; LOW LEVEL
1 ; HIGH LEVEL

TC4S69F (TOSHIBA) FLAT PACKAGE

C-MOS INVERTER BUFFER

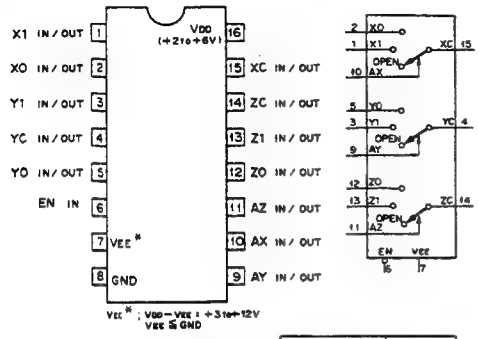
– TOP VIEW –



TC74HC4053AF (TOSHIBA) FLAT PACKAGE

C-MOS TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

– TOP VIEW –



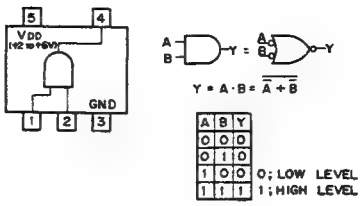

| CONT. INPUTS | | ON |
|---|---|---|
| EN | A (X,Y,Z) | CHANNEL |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | X | OPEN |

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE.

TC7S08F (TOSHIBA) FLAT PACKAGE

C-MOS 2-INPUT AND GATE

– TOP VIEW –



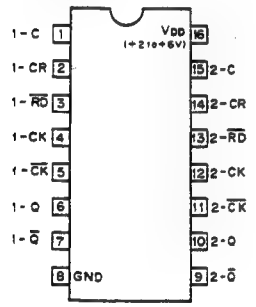

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

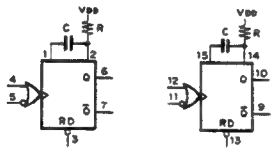
0 ; LOW LEVEL
1 ; HIGH LEVEL

TC74HC4538AF (TOSHIBA) FLAT PACKAGE

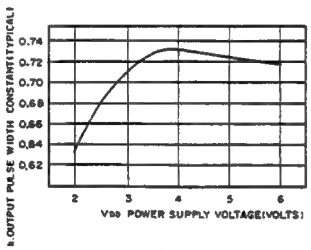
C - MOS DUAL RETRIGGERABLE / NON - RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

– TOP VIEW –



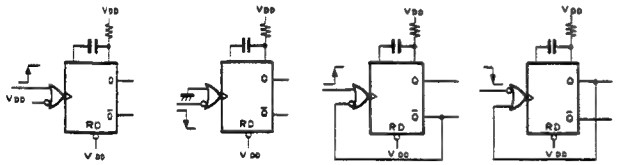




OUTPUT PULSE WIDTH = k·C·R




RETRIGGERABLE M.M.V

NON-RETRIGGERABLE M.M.V



# SECTION C
# SPARE PARTS

## C-1. PARTS INFORMATION

1. **Safety Related Component Warning**

   Components indentified by shading marked with ⚠ on the schematic diagrams, exploded views and electrical spare parts list are critical to safe operation. Replace these components with Sony parts whose parts numbers appear as shown in this manual or in service manual supplements published by Sony.

2. Replacement Parts supplied from Sony Parts Center will sometimes have different shape and outside view from the parts which actually in use. This is due to **"accommodating the improved parts and/or engineering changes" or "standardization of genuine parts."** This manual 's exploded view and electrical spare parts lists are indicating the parts numbers of "the standardized genuine parts at present." Regarding engineering parts and diagrams changes in our engineering department, refer to SONY service bulletins and service manual supplements.

3. The parts marked with "S" in the SP column of the exploded views and electrical spare parts list are normally required for routine service work. Orders for parts marked with "O" will be processed, but allow for additional delivery time.

4. Item with no parts number and/or no description are not stocked because they are seldom required for routine service.

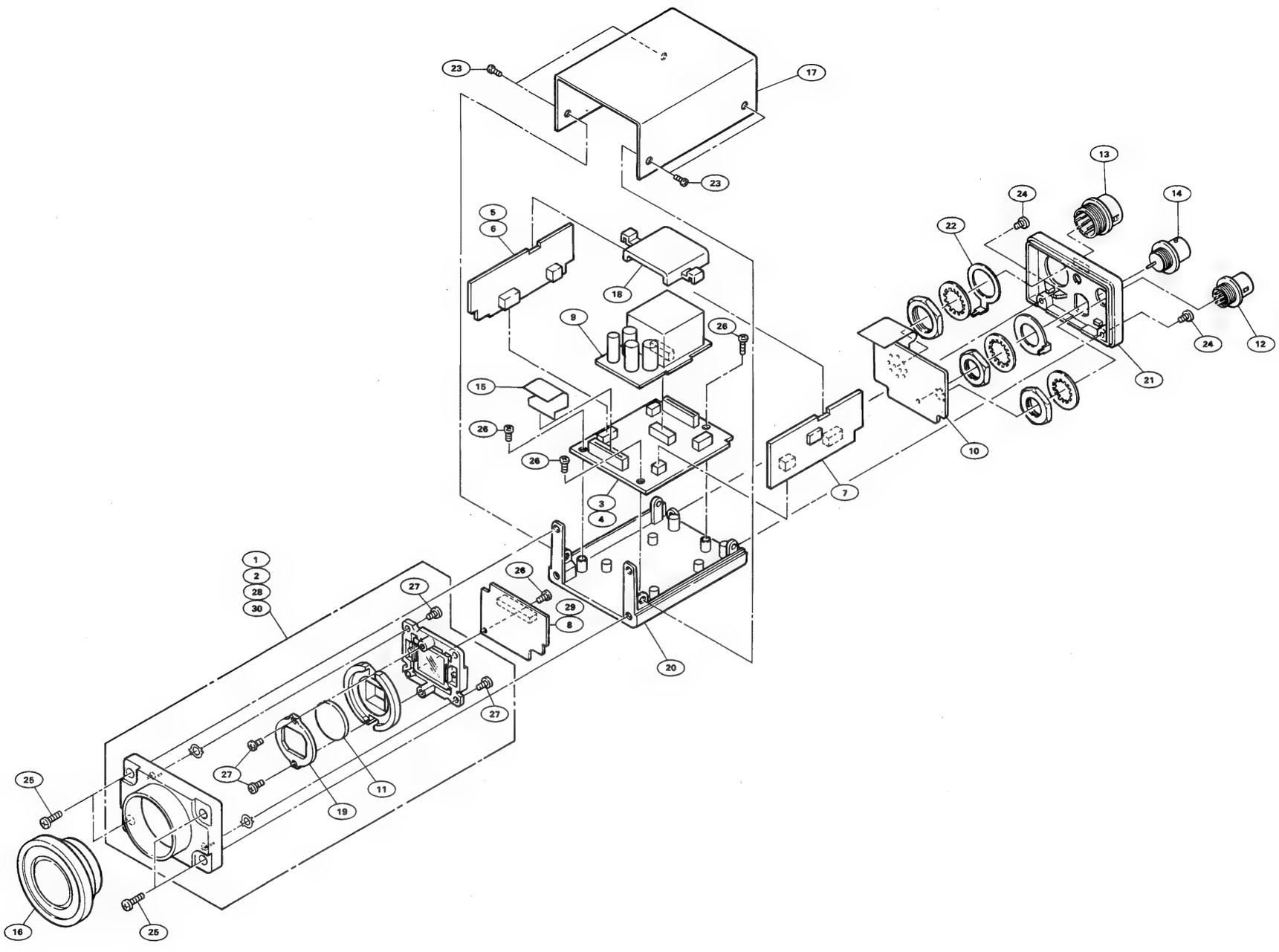
5. All capacitors are in micro farads unless otherwise specified.
   All inductors are in micro henries unless otherwise specified.
   All resistors are in ohms.

## C-2. EXPLODED VIEW

| No. | Part No. | SP | Description |
|---|---|---|---|
| 1 | A-7575-194-A | s | CCD UNIT-XC75(N) (for XC-75) |
| 2 | A-7575-195-A | s | CCD UNIT-XC75CE(P) (for XC-75CE) |
| 3 | A-8271-185-A | o | MOUNTED CIRCUIT BOARD, MB-403 (for XC-75/73) |
| 4 | A-8271-186-A | o | MOUNTED CIRCUIT BOARD, MB-403P (for XC-75CE/73CE) |
| 5 | A-8271-187-A | o | MOUNTED CIRCUIT BOARD, SG-199 (for XC-75/73) |
| 6 | A-8271-188-A | o | MOUNTED CIRCUIT BOARD, SG-199P (for XC-75CE/73CE) |
| 7 | A-8271-189-A | o | MOUNTED CIRCUIT BOARD, PR-165 |
| 8 | A-8276-210-A | o | MOUNTED CIRCUIT BOARD, PA-147 (for XC-75/75CE) |
| 9 | A-8276-211-A | o | MOUNTED CIRCUIT BOARD, PS-268 |
| 10 | A-8276-212-A | o | MOUNTED CIRCUIT BOARD, CN-649 |
| 11 | 1-547-185-31 | o | FILTER, INFRARED CUT |
| 12 | 1-562-222-21 | s | CONNECTOR, 6P FEMALE "LENS" |
| 13 | 1-562-381-00 | s | CONNECTOR, 12P MALE "DC IN/SYNC" |
| 14 | 1-580-724-21 | s | CONNECTOR, BNC "VIDEO OUT" |
| 15 | 1-642-810-11 | s | WIRE, FLEXIBLE CARD, 20P, HN-179 |
| 16 | 2-042-385-00 | s | CAP, C MOUNT |
| 17 | 3-174-880-01 | o | CASE, UPPER |
| 18 | 3-174-882-01 | s | RUBBER, RADIATION |
| 19 | 3-174-883-01 | o | BRACKET, FILTER |
| 20 | 3-175-341-04 | o | CHASSIS |
| 21 | 3-175-342-01 | o | PANEL, REAR |
| 22 | 3-718-804-01 | o | LUG, GROUND |
| 23 | 3-719-381-01 | s | SCREW M2X4 |
| 24 | 7-628-254-10 | s | SCREW +PS 2.6X6 |
| 25 | 7-621-775-40 | s | SCREW +B 2.6X8 |
| 26 | 7-627-553-47 | s | PRECISION SCREW +P 2X4 TYPE 1 |
| 27 | 7-627-853-48 | s | PRECISION SCREW +P 2X4 TYPE 3 |
| 28 | A-7575-207-A | s | CCD UNIT-XC73(N) (for XC-73) |
| 29 | A-8276-382-A | o | MOUNTED CIRCUIT BOARD, PA-152 (for XC-73/73CE) |
| 30 | A-7575-208-A | s | CCD UNIT-XC73CE(P) (for XC-73CE) |

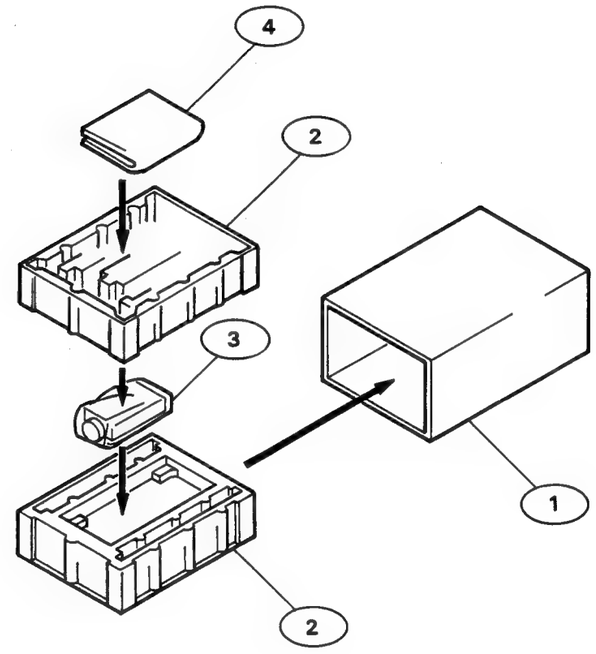
## EXPLODED VIEW

EXPLODED VIEW



## C-3. PACKING MATERIALS AND SUPPLIED ACCESSORY

| No. | | Part No. | SP | Description |
|---|---|---|---|---|
| 1 | | 3-176-140-01 | o | INDIVIDUAL CARTON (for XC-75) |
| | | 3-176-141-01 | o | INDIVIDUAL CARTON (for XC-75CE) |
| | | 3-177-021-01 | o | INDIVIDUAL CARTON (for XC-73) |
| | | 3-179-074-01 | o | INDIVIDUAL CARTON (for XC-73CE) |
| 2 | | 3-176-144-01 | o | CUSHION |
| 3 | | 3-338-735-01 | o | BAG (STANDARD), PROTECTION |
| 4 | ⚠ | 3-754-795-12 | s | MANUAL, INSTRUCTION (XC-75/75CE) |
| | ⚠ | 3-755-368-12 | s | MANUAL, INSTRUCTION (XC-73/73CE) |



# C-4. ELECTRICAL PARTS LIST

CN-649 BOARD

| Ref. No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| 1pc | A-8276-212-A | o | MOUNTED CIRCUIT BOARD, CN-649 |
| C1 | 1-162-919-11 | s | CERAMIC, CHIP 22PF 5% 50V |
| C2 | 1-162-915-11 | s | CERAMIC, CHIP 10PF 5PF 50V |
| C3 | 1-162-919-11 | s | CERAMIC, CHIP 22PF 5% 50V |
| C4 | 1-162-926-11 | s | CERAMIC, CHIP 82PF 5% 50V |
| C5 | 1-164-156-11 | s | CERAMIC 0.1uF 25V |
| C6 | 1-162-957-11 | s | CERAMIC 220PF 5% 50V |
| C7 | 1-162-927-11 | s | CERAMIC, CHIP 100PF 5% 50V |
| C8 | 1-164-156-11 | s | CERAMIC 0.1uF 25V |
| C9 | 1-135-208-11 | s | TANTALUM 1uF 20% 10V |
| D1 | 8-719-510-11 | s | DIODE D1FS4 |
| F1 | ⚠1-576-220-21 | s | FUSE, CHIP |
| L1 | 1-410-981-31 | s | INDUCTOR CHIP 0.1UH |
| L2 | 1-410-995-41 | s | INDUCTOR CHIP 1.5uH |
| L3 | 1-412-780-41 | s | INDUCTOR 2.2UH |
| L4 | 1-410-981-31 | s | INDUCTOR CHIP 0.1UH |
| L5 | 1-410-981-31 | s | INDUCTOR CHIP 0.1UH |
| L6 | 1-410-981-31 | s | INDUCTOR CHIP 0.1UH |
| R1 | 1-216-830-11 | s | METAL, CHIP 5.6K 5% 1/16W |
| R2 | 1-216-828-11 | s | METAL, CHIP 3.9K 5% 1/16W |
| R3 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R4 | 1-216-821-11 | s | METAL, CHIP 1K 5% 1/16W |
| RV1 | 1-237-605-11 | s | RES, ADJ, 10K |
| S1 | 1-554-945-21 | s | SWITCH, SLIDE |

MB-403 BOARD

| Ref. No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| 1pc | A-8271-185-A | o | MOUNTED CIRCUIT BOARD, MB-403 (for XC-73/75) |
| 1pc | A-8271-186-A | o | MOUNTED CIRCUIT BOARD, MB-403P (for XC-73CE/75CE) |
| C1 | 1-135-076-21 | s | TANTALUM, CHIP 1uF 10% 35V |
| C2 | 1-135-076-21 | s | TANTALUM, CHIP 1uF 10% 35V |
| C3 | 1-135-076-21 | s | TANTALUM, CHIP 1uF 10% 35V |
| C4 | 1-135-165-11 | s | TANTALUM 33uF 10% 16V |
| C5 | 1-135-217-21 | s | TANTALUM 15uF 20% 6.3V |
| C6 | 1-162-907-11 | s | CERAMIC, CHIP 2PF 50V |
| C7 | 1-135-214-21 | s | TANTALUM 4.7uF 20% 20V |
| C8 | 1-135-215-21 | s | TANTALUM 6.8uF 20% 16V |
| C9 | 1-162-908-11 | s | CERAMIC 3PF 0.25PF 50V |
| C10 | 1-164-156-11 | s | CERAMIC 0.1uF 25V |

(MB-403 BOARD)

| Ref. No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| C11 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C12 | 1-135-217-21 | s | TANTALUM 15uF 20% 6.3V |
| C13 | 1-135-211-11 | s | TANTALUM 6.8uF 20% 6.3V |
| C14 | 1-135-157-21 | s | TANTALUM 10uF 10% 6.3V |
| C15 | 1-135-227-11 | s | TANTALUM 100uF 20% 6.3V |
| C16 | 1-164-156-11 | s | CERAMIC 0.1uF 25V |
| C17 | 1-162-964-11 | s | CERAMIC 0.001uF 10% 50V |
| C18 | 1-162-919-11 | s | CERAMIC, CHIP 22PF 5% 50V |
| C19 | 1-162-915-11 | s | CERAMIC, CHIP 10PF 5PF 50V |
| C20 | 1-162-915-11 | s | CERAMIC, CHIP 10PF 5PF 50V |
| C22 | 1-135-211-11 | s | TANTALUM 6.8uF 20% 6.3V |
| C23 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C24 | 1-162-927-11 | s | CERAMIC, CHIP 100PF 5% 50V |
| C25 | 1-162-915-11 | s | CERAMIC, CHIP 10PF 5PF 50V |
| C26 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C27 | 1-164-156-11 | s | CERAMIC 0.1uF 25V<br>Ser.No. 10001 to 10600 for XC-75<br>Ser.No. 10001 to 10200 for XC-75CE |
| | 1-164-227-11 | s | CERAMIC, CHIP 0.022uF 10% 25V<br>Ser.No. 10001 and up for XC-73<br>Ser.No. 400001 and up for XC-73CE<br>Ser.No. 10601 and up for XC-75<br>Ser.No. 10201 and up for XC-75CE |
| C28 | 1-162-917-11 | s | CERAMIC, CHIP 15PF 5% 50V<br>Ser.No. 10001 to 12530 for XC-73<br>Ser.No. 400001 to 400830 for XC-73CE<br>Ser.No. 10001 to 42750 for XC-75<br>Ser.No. 10001 to 20050 for XC-75CE |
| | 1-162-916-11 | s | CERAMIC, CHIP 12PF 5% 50V<br>Ser.No. 12531 and up for XC-73<br>Ser.No. 400831 and up for XC-73CE<br>Ser.No. 42751 and up for XC-75<br>Ser.No. 20051 and up for XC-75CE |
| C29 | 1-162-915-11 | s | CERAMIC, CHIP 10PF 0.5PF 50V<br>Ser.No. 10001 to 10750 for XC-73<br>Ser.No. 400001 to 400100 for XC-73CE<br>Ser.No. 10151 to 24500 for XC-75<br>Ser.No. 10051 to 14150 for XC-75CE |
| | 1-162-911-11 | s | CERAMIC, CHIP 6PF 0.5PF 50V<br>Ser.No. 10751 and up for XC-73<br>Ser.No. 400201 and up for XC-73CE<br>Ser.No. 24501 and up for XC-75<br>Ser.No. 14151 and up for XC-75CE |
| C30 | 1-162-975-11 | s | CERAMIC 24PF 5% 50V |
| C31 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V<br>Ser.No. 10001 to 11271 for XC-73<br>Ser.No. 400001 to 400300 for XC-73CE<br>Ser.No. 10001 to 31801 for XC-75<br>Ser.No. 10001 to 17701 for XC-75CE |
| | 1-162-927-11 | s | CERAMIC, CHIP 100PF 5% 50V<br>Ser.No. 11271 and up for XC-73<br>Ser.No. 400301 and up for XC-73CE<br>Ser.No. 31801 and up for XC-75<br>Ser.No. 17701 and up for XC-75CE |

(MB-403 BOARD)

| Ref. No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| C32 | 1-162-927-11 | s | CERAMIC, CHIP 100PF 5% 50V |
| C33 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C34 | 1-135-190-21 | s | TANTALUM 0.1uF 20% 20V |
| C35 | 1-135-217-21 | s | TANTALUM 15uF 20% 6.3V |
| C36 | 1-135-097-21 | s | TANTALUM, CHIP 15uF 10% 10V |
| C37 | 1-135-227-11 | s | TANTALUM 100uF 20% 6.3V |
| C38 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C39 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C40 | 1-135-076-21 | s | TANTALUM, CHIP 1uF 10% 35V |
| C41 | 1-164-156-11 | s | CERAMIC 0.1uF 25V |
| C42 | 1-164-156-11 | s | CERAMIC 0.1uF 25V |
| C43 | 1-162-915-11 | s | CERAMIC, CHIP 10PF 0.5PF 50V |
| C44 | 1-135-180-21 | s | TANTALUM 3.3uF 20% 6.3V |
| C45 | *1-162-905-11 | s | CERAMIC 1PF 0.25PF 50V |
| | *1-162-907-11 | s | CERAMIC 2PF 0.25PF 50V |
| | *1-162-908-11 | s | CERAMIC 3PF 0.25PF 50V |
| | *CHOICE | | |
| CN1 | 1-568-331-11 | s | CONNECTOR, 10P MALE |
| CN2 | 1-568-330-41 | s | CONNECTOR, 6P MALE |
| CN3 | 1-691-630-21 | ◘ | CONNECTOR, FFC/FPC (ZIF) 20P |
| CN4 | 1-568-334-41 | s | CONNECTOR, 16P MALE |
| CN5 | 1-691-630-21 | ◘ | CONNECTOR, FFC/FPC (ZIF) 20P |
| CN6 | 1-568-330-41 | s | CONNECTOR, 6P MALE |
| CN7 | 1-568-331-11 | s | CONNECTOR, 10P MALE |
| CT1 | 1-141-423-61 | s | CAP, TRIMMER |
| D1 | 8-719-820-05 | s | DIODE 1SS181 |
| D2 | 8-719-820-05 | s | DIODE 1SS181 |
| D3 | 8-719-820-05 | s | DIODE 1SS181 |
| D4 | 8-719-820-05 | s | DIODE 1SS181 |
| D5 | 8-719-974-98 | s | DIODE HVM17-01 |
| D6 | 8-719-820-05 | s | DIODE 1SS181 |
| D7 | 8-719-820-05 | s | DIODE 1SS181 |
| FL1 | 1-409-496-21 | s | FILTER, LC TRAP |
| FL2 | 1-409-496-21 | s | FILTER, LC TRAP |
| IC1 | 8-752-327-48 | s | IC CXD1250N |
| IC2 | 8-759-032-01 | s | IC MC74HC00AF |
| IC3 | 8-752-351-03 | s | IC CXD1256AR |
| IC4 | 8-759-925-74 | s | IC SN74HC04ANS |
| IC5 | 8-759-925-83 | s | IC SN74HC27NS |
| IC6 | 8-759-239-34 | s | IC TC74HC4538AF |
| L1 | 1-412-788-41 | s | INDUCTOR 10UH |
| L2 | 1-412-784-41 | s | INDUCTOR 4.7UH |
| L3 | 1-412-780-41 | s | INDUCTOR 2.2UH |
| L4 | 1-412-780-41 | s | INDUCTOR 2.2UH |
| L5 | 1-410-997-31 | s | INDUCTOR CHIP 2.2UH |
| L6 | 1-412-177-21 | s | INDUCTOR 2.2UH |
| L7 | 1-412-792-41 | s | INDUCTOR 22UH |
| L8 | 1-412-788-41 | s | INDUCTOR 10UH |
| Q1 | 8-729-926-19 | s | TRANSISTOR 2SC4103-Q |
| Q2 | 8-729-117-16 | s | TRANSISTOR 2SA1611-M6 |
| Q3 | 8-729-427-74 | s | TRANSISTOR XP4601 |
| Q4 | 8-729-122-63 | s | TRANSISTOR 2SA1226 |
| Q5 | 8-729-175-73 | s | TRANSISTOR 2SC2757 |
| Q6 | 8-729-117-16 | s | TRANSISTOR 2SA1611-M6 |
| Q7 | 8-729-926-19 | s | TRANSISTOR 2SC4103-Q |
| Q8 | 8-729-117-32 | s | TRANSISTOR 2SC4177 |
| Q9 | 8-729-427-74 | s | TRANSISTOR XP4601 |

(MB-403 BOARD)

| Ref. No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| Q10 | 8-729-117-16 | s | TRANSISTOR 2SA1611-M6 |
| Q11 | 8-729-117-32 | s | TRANSISTOR 2SC4177 |
| Q12 | 8-729-427-83 | s | TRANSISTOR XP6501 |
| Q13 | 8-729-117-32 | s | TRANSISTOR 2SC4177 |
| Q14 | 8-729-427-74 | s | TRANSISTOR XP4601 |
| R1 | 1-216-845-11 | s | METAL, CHIP 100K 5% 1/16W |
| R2 | 1-216-821-11 | s | METAL, CHIP 1K 5% 1/16W |
| R3 | 1-216-840-11 | s | METAL, CHIP 39K 5% 1/16W |
| R4 | 1-216-829-11 | s | METAL, CHIP 4.7K 5% 1/16W |
| R5 | 1-216-823-11 | s | METAL, CHIP 1.5K 5% 1/16W |
| R6 | 1-216-817-11 | s | METAL, CHIP 470 5% 1/16W |
| R7 | 1-216-829-11 | s | METAL, CHIP 4.7K 5% 1/16W |
| R8 | 1-216-795-11 | s | METAL, CHIP 6.8K 0.50% 1/16W |
| R9 | 1-218-708-11 | s | METAL, FILM CHIP 4.7K 0.50% 1/16W |
| R10 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R11 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W (for XC-73/75) |
| R12 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W (for XC-73CE/75CE) |
| R13 | 1-216-834-11 | s | METAL, CHIP 12K 5% 1/16W |
| R14 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R15 | 1-216-797-11 | s | METAL, CHIP 10 5% 1/16W |
| R16 | 1-216-797-11 | s | METAL, CHIP 10 5% 1/16W |
| R17 | 1-216-835-11 | s | METAL, CHIP 15K 5% 1/16W |
| R18 | 1-216-623-11 | s | METAL, CHIP 68 0.5% 1/10W |
| R19 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R20 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R21 | 1-216-813-11 | s | METAL, CHIP 220 5% 1/16W |
| R22 | 1-216-801-11 | s | METAL, CHIP 22 5% 1/16W |
| R23 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R24 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R25 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R26 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R27 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R28 | 1-216-813-11 | s | METAL, CHIP 220 5% 1/16W |
| R29 | 1-216-813-11 | s | METAL, CHIP 220 5% 1/16W |
| R30 | 1-216-809-11 | s | METAL, CHIP 100 5% 1/16W |
| R31 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R32 | 1-216-857-11 | s | METAL, CHIP 1M 5% 1/16W |
| R33 | 1-216-851-11 | s | METAL, CHIP 330K 5% 1/16W<br>Ser.No. 10001 to 10600 for XC-75<br>Ser.No. 10001 to 10200 for XC-75CE |
| | 1-216-856-11 | s | RES, CHIP 820K 5% 1/16W<br>Ser.No. 10001 and up for XC-73<br>Ser.No. 400001 and up for XC-73CE<br>Ser.No. 10601 and up for XC-75<br>Ser.No. 10201 and up for XC-75CE |
| R34 | 1-216-857-11 | s | METAL, CHIP 1M 5% 1/16W |
| R35 | 1-216-829-11 | s | METAL, CHIP 4.7K 5% 1/16W |
| R36 | 1-216-837-11 | s | METAL, CHIP 22K 5% 1/16W |
| R37 | 1-216-839-11 | s | METAL, CHIP 33K 5% 1/16W |
| R38 | 1-216-845-11 | s | METAL, CHIP 100K 5% 1/16W |
| R39 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R40 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R41 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R42 | 1-216-797-11 | s | METAL, CHIP 10 5% 1/16W |
| R43 | 1-216-797-11 | s | METAL, CHIP 10 5% 1/16W |

(MB-403/403P BOARD)

| Ref. No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| R44 | 1-216-623-11 | s | METAL, CHIP 68 0.5% 1/10W |
| R45 | 1-216-857-11 | s | METAL, CHIP 1M 5% 1/16W |
| R46 | 1-216-835-11 | s | METAL, CHIP 15K 5% 1/16W |
| R47 | 1-216-835-11 | s | METAL, CHIP 15K 5% 1/16W |
| R48 | 1-216-840-11 | s | METAL, CHIP 39K 5% 1/16W |
| R49 | 1-216-850-11 | s | METAL, CHIP 270K 5% 1/16W |
| R50 | 1-216-842-11 | s | METAL, CHIP 56K 5% 1/16W |
| R51 | 1-216-838-11 | s | METAL, CHIP 27K 5% 1/16W |
| R52 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R53 | 1-216-864-11 | s | METAL, CHIP 0-OHM |
| R54 | 1-216-841-11 | s | METAL, CHIP 47K 5% 1/16W |
| R55 | 1-216-827-11 | s | METAL, CHIP 3.3K 5% 1/16W |
| R56 | 1-216-829-11 | s | METAL, CHIP 4.7K 5% 1/16W |
| R57 | 1-216-829-11 | s | METAL, CHIP 4.7K 5% 1/16W |
| R58 | 1-216-821-11 | s | METAL, CHIP 1K 5% 1/16W |
| R59 | 1-216-809-11 | s | METAL, CHIP 100 5% 1/16W |
| R60 | 1-216-840-11 | s | METAL, CHIP 39K 5% 1/16W |
| R61 | 1-216-821-11 | s | METAL, CHIP 1K 5% 1/16W |
| RV1 | 1-238-092-11 | s | RES, ADJ, 47K |
| RV2 | 1-238-091-11 | s | RES, ADJ, 22K |
| S1 | 1-692-066-21 | s | SWITCH, ROTARY |
| X1 | 1-579-619-11 | s | CRYSTAL 28.636363MHz (for XC-73/75) |
| | 1-579-621-11 | s | CRYSTAL 28.3750MHz (for XC-73CE/75CE) |

PA-147 BOARD (FOR XC-73/73CE)

| Ref. No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| 1pc | A-8276-210-A | o | MOUNTED CIRCUIT BOARD, PA-147 (for XC-75/75CE) |
| C1 | 1-135-162-21 | s | TANTAL 33uF 10% 6.3V |
| C2 | 1-135-159-21 | s | TANTALUM, CHIP 10uF 10% 20V |
| C3 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C4 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C5 | 1-135-076-21 | s | TANTALUM, CHIP 1uF 10% 35V |
| C6 | 1-135-164-21 | s | TANTALUM 22uF 20% 10V |
| C7 | 1-162-964-11 | s | CERAMIC 0.001uF 10% 50V |
| C8 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C9 | 1-135-161-21 | s | TANTALUM, CHIP 22uF 10% 10V |
| C10 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C11 | 1-135-162-21 | s | TANTALUM 33uF 10% 6.3V |
| C12 | 1-164-156-11 | s | CERAMIC 0.1uF 25V |
| CN1 | 1-691-630-21 | o | CONNECTOR, FFC/FPC (ZIF) 20P |
| IC2 | 8-752-052-72 | s | IC CXA1439M |
| Q1 | 8-729-117-16 | s | TRANSISTOR 2SA1611-M6 |
| Q2 | 8-729-117-16 | s | TRANSISTOR 2SA1611-M6 |
| Q3 | 8-729-926-19 | s | TRANSISTOR 2SC4103-Q |
| Q4 | 8-729-429-98 | s | TRANSISTOR XP1401 |
| R1 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R2 | 1-216-827-11 | s | METAL, CHIP 3.3K 5% 1/16W |
| R3 | 1-216-835-11 | s | METAL, CHIP 15K 5% 1/16W |
| R4 | 1-216-822-11 | s | METAL, CHIP 1.2K 5% 1/16W |
| R5 | 1-216-838-11 | s | METAL, CHIP 27K 5% 1/16W |
| R6 | 1-216-848-11 | s | METAL, CHIP 180K 5% 1/16W |
| R7 | 1-216-837-11 | s | METAL, CHIP 22K 5% 1/16W |
| R8 | 1-216-845-11 | s | METAL, CHIP 100K 5% 1/16W |

## PA-152 BOARD (FOR XC-73/73CE)

| Ref. No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| 1pc | A-8276-382-A | ◻ | MOUNTED CIRCUIT BOARD, PA-152 (for XC-73/73CE) |
| C1 | 1-135-246-11 | s | TANTALUM 33uF 20% 6.3V |
| C2 | 1-135-159-21 | s | TANTALUM, CHIP 10uF 10% 20V |
| C3 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C4 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C5 | 1-135-324-11 | s | TANTALUM, CHIP 1uF 20% 20V |
| C6 | 1-135-164-21 | s | TANTALUM 22uF 20% 10V |
| C7 | 1-162-964-11 | s | CERAMIC 0.001uF 10% 50V |
| C8 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C9 | 1-135-245-11 | s | TANTALUM, CHIP 22uF 20% 6.3V |
| C10 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C11 | 1-135-246-11 | s | TANTALUM 33uF 20% 6.3V |
| C12 | 1-164-156-11 | s | CERAMIC 0.1uF 25V |
| CN1 | 1-691-630-21 | ◻ | CONNECTOR, FFC/FPC (ZIF) 20P |
| IC2 | 8-752-052-72 | s | IC CXA1439M |
| Q1 | 8-729-117-16 | s | TRANSISTOR 2SA1611-M6 |
| Q2 | 8-729-429-98 | s | TRANSISTOR XP1401 |
| Q3 | 8-729-926-19 | s | TRANSISTOR 2SC4103-Q |
| R1 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R2 | 1-216-827-11 | s | METAL, CHIP 3.3K 5% 1/16W |
| R3 | 1-216-845-11 | s | METAL, CHIP 100K 5% 1/16W |
| R4 | 1-216-820-11 | s | METAL, CHIP 820 5% 1/16W |
| R5 | 1-216-843-11 | s | METAL, CHIP 68K 5% 1/16W |
| R6 | 1-216-848-11 | s | METAL, CHIP 180K 5% 1/16W |
| R7 | 1-216-837-11 | s | METAL, CHIP 22K 5% 1/16W |

## PR-165 BOARD

| Ref. No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| 1pc | A-8271-189-A | ◻ | MOUNTED CIRCUIT BOARD, PR-165 |
| C1 | 1-135-227-11 | s | TANTALUM 100uF 20% 6.3V |
| C2 | 1-135-157-21 | s | TANTALUM 10uF 10% 6.3V |
| C3 | 1-135-208-11 | s | TANTALUM 1uF 20% 10V |
| C4 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C5 | 1-162-927-11 | s | CERAMIC, CHIP 100PF 5% 50V |
| C6 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C7 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C8 | 1-162-910-11 | s | CERAMIC 5PF 0.25PF 50V |
| C9 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C10 | 1-135-201-11 | s | TANTALUM 10uF 20% 6.3V |
| C11 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C12 | 1-135-217-21 | s | TANTALUM 15uF 20% 6.3V |
| C13 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C14 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C15 | 1-135-149-21 | s | TANTALUM, CHIP 2.2uF 10% 10V |
| C16 | 1-135-149-21 | s | TANTALUM, CHIP 2.2uF 10% 10V |
| C17 | 1-164-156-11 | s | CERAMIC 0.1uF 25V |
| C18 | 1-135-208-11 | s | TANTALUM 1uF 20% 10V |
| C19 | 1-135-208-11 | s | TANTALUM 1uF 20% 10V |
| C20 | 1-135-208-11 | s | TANTALUM 1uF 20% 10V |
| C21 | 1-135-227-11 | s | TANTALUM 100uF 20% 6.3V |
| C22 | 1-135-211-11 | s | TANTALUM 6.8uF 20% 6.3V |
| C23 | 1-135-210-11 | s | TANTALUM 4.7uF 10% 10V |
| C24 | 1-162-915-11 | s | CERAMIC, CHIP 10PF 5PF 50V |
| C25 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C26 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C27 | 1-135-149-21 | s | TANTALUM, CHIP 2.2uF 10% 10V |
| CN1 | 1-568-362-41 | s | CONNECTOR, 6P FEMALE |
| CN2 | 1-568-363-31 | s | CONNECTOR, 10P FEMALE |
| IC1 | 8-752-230-99 | s | IC TC74HC4053AF |
| IC2 | 8-752-051-25 | s | IC CXA1310AQ |
| IC3 | 8-752-230-99 | s | IC TC74HC4053AF |
| L1 | 1-412-780-41 | s | INDUCTOR 2.2UH |
| Q1 | 8-729-117-32 | s | TRANSISTOR 2SC4177 |
| Q2 | 8-729-117-32 | s | TRANSISTOR 2SC4177 |
| Q3 | 8-729-926-19 | s | TRANSISTOR 2SC4103-Q |
| Q4 | 8-729-427-83 | s | TRANSISTOR XP6501 |
| Q5 | 8-729-117-32 | s | TRANSISTOR 2SC4177 |
| Q6 | 8-729-117-32 | s | TRANSISTOR 2SC4177 |
| Q7 | 8-729-427-74 | s | TRANSISTOR XP4601 |
| Q8 | 8-729-117-32 | s | TRANSISTOR 2SC4177 |
| Q9 | 8-729-117-32 | s | TRANSISTOR 2SC4177 |
| Q10 | 8-729-117-16 | s | TRANSISTOR 2SA1611-M6 |
| Q11 | 8-729-117-16 | s | TRANSISTOR 2SA1611-M6 |
| R1 | 1-216-864-11 | s | METAL, CHIP 0-OHM |
| R2 | 1-218-716-11 | s | METAL 10K 0.50% 1/16W |
| R3 | 1-218-716-11 | s | METAL 10K 0.50% 1/16W |
| R4 | 1-218-716-11 | s | METAL 10K 0.50% 1/16W |
| R5 | 1-216-817-11 | s | METAL, CHIP 470 5% 1/16W |
| R6 | 1-216-817-11 | s | METAL, CHIP 470 5% 1/16W |
| R7 | 1-218-716-11 | s | METAL 10K 0.50% 1/16W |
| R8 | 1-218-680-11 | s | METAL 330 0.50% 1/16W |
| R9 | 1-218-680-11 | s | METAL 330 0.50% 1/16W |
| R10 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |

(PR-165 BOARD)

| Ref. No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| R11 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R12 | 1-218-716-11 | s | METAL 10K 0.50% 1/16W |
| R13 | 1-218-716-11 | s | METAL 10K 0.50% 1/16W |
| R14 | 1-216-821-11 | s | METAL, CHIP 1K 5% 1/16W |
| R15 | 1-216-831-11 | s | METAL, CHIP 6.8K 5% 1/16W |
| R16 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R17 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R18 | 1-216-837-11 | s | METAL, CHIP 22K 5% 1/16W |
| R19 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R20 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R21 | 1-216-837-11 | s | METAL, CHIP 22K 5% 1/16W |
| R22 | 1-216-829-11 | s | METAL, CHIP 4.7K 5% 1/16W |
| R23 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R24 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R25 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R26 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R27 | 1-216-845-11 | s | METAL, CHIP 100K 5% 1/16W |
| R28 | 1-216-815-11 | s | METAL, CHIP 330 5% 1/16W |
| R29 | 1-216-857-11 | s | METAL, CHIP 1M 5% 1/16W |
| R30 | 1-216-827-11 | s | METAL, CHIP 3.3K 5% 1/16W |
| R31 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R32 | 1-216-827-11 | s | METAL, CHIP 3.3K 5% 1/16W |
| R33 | 1-216-829-11 | s | METAL, CHIP 4.7K 5% 1/16W |
| R34 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R35 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R36 | 1-216-815-11 | s | METAL, CHIP 330 5% 1/16W |
| R37 | 1-216-829-11 | s | METAL, CHIP 4.7K 5% 1/16W |
| R38 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R39 | 1-216-831-11 | s | METAL, CHIP 6.8K 5% 1/16W |
| R40 | 1-216-829-11 | s | METAL, CHIP 4.7K 5% 1/16W |
| R41 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R42 | 1-216-831-11 | s | METAL, CHIP 6.8K 5% 1/16W |
| R43 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R44 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R45 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R46 | 1-216-829-11 | s | METAL, CHIP 4.7K 5% 1/16W |
| R47 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R48 | 1-216-821-11 | s | METAL, CHIP 1K 5% 1/16W |
| RV1 | 1-241-833-21 | s | RES, ADJ, CHIP 10K |
| RV2 | 1-241-828-21 | s | RES, ADJ, CHIP 500 |
| RV3 | 1-241-829-21 | s | RES, ADJ, CHIP 1K |
| RV4 | 1-241-833-21 | s | RES, ADJ, CHIP 10K |
| RV5 | 1-238-090-11 | s | RES, ADJ, 10K |
| RV6 | 1-238-088-11 | s | RES, ADJ, 2.2K |
| RV7 | 1-238-087-11 | s | RES, ADJ, 1K |
| RV8 | 1-238-090-11 | s | RES, ADJ, 10K |
| RV9 | 1-238-088-11 | s | RES, ADJ, 2.2K |
| RV10 | 1-238-089-11 | s | RES, ADJ, 4.7K |
| S1 | *1-571-249-11 | s | SWITCH, SLIDE |
| | *DELETED | | Ser.No. 15551 and up for XC-73 |
| | | | Ser.No. 405151 and up for XC-73CE |
| | | | Ser.No. 60901 and up for XC-75 |
| | | | Ser.No. 53001 and up for XC-75CE |

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PS-268 BOARD

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| Ref. No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| 1pc | A-8276-211-A | o | MOUNTED CIRCUIT BOARD, PS-268 |
| C101 | 1-135-161-21 | s | TANTALUM, CHIP 22uF 10% 10V |
| C102 | 1-164-156-11 | s | CERAMIC 0.1uF 25% |
| C103 | 1-126-947-11 | s | ELECT 47uF 20% 35V |
| C104 | 1-135-161-21 | s | TANTALUM, CHIP 22uF 10% 10V |
| C105 | 1-126-925-11 | s | ELECT 470uF 20% 10V |
| C106 | 1-126-925-11 | s | ELECT 470uF 20% 10V |
| C107 | 1-126-948-11 | s | ELECT 100uF 20% 35V |
| C108 | 1-135-161-21 | s | TANTALUM, CHIP 22uF 10% 10V |
| CN101 | 1-568-357-11 | s | CONNECTOR, 16P FEMALE |
| L101 | 1-412-060-11 | s | INDUCTOR CHIP 22UH |
| L102 | 1-412-060-11 | s | INDUCTOR CHIP 22UH |
| L103 | 1-412-034-11 | s | INDUCTOR CHIP 330UH |
| L104 | 1-412-034-11 | s | INDUCTOR CHIP 330UH |
| L105 | 1-412-060-11 | s | INDUCTOR CHIP 22UH |
| PU101 | 1-466-694-11 | s | CONVERTER, DC-DC |
| Q101 | 8-729-117-32 | s | TRANSISTOR 2SC4177 |
| Q102 | 8-729-216-22 | s | TRANSISTOR 2SA1162 |
| R101 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R102 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R103 | 1-216-829-11 | s | METAL, CHIP 4.7K 5% 1/16W |

SG-199 BOARD

| Ref. No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| 1pc | A-8271-187-A | ◎ | MOUNTED CIRCUIT BOARD, SG-199 (for XC-73/75) |
| 1pc | A-8271-188-A | ◎ | MOUNTED CIRCUIT BOARD, SG-199P (for XC-73CE/75CE) |
| C1 | 1-135-227-11 | s | TANTALUM 100uF 20% 6.3V |
| C2 | 1-162-919-11 | s | CERAMIC, CHIP 22PF 5% 50V |
| C3 | 1-162-919-11 | s | CERAMIC, CHIP 22PF 5% 50V |
| C4 | 1-162-919-11 | s | CERAMIC, CHIP 22PF 5% 50V |
| C5 | 1-162-923-11 | s | CERAMIC, CHIP 47PF 5% 50V |
| C6 | 1-162-923-11 | s | CERAMIC, CHIP 47PF 5% 50V |
| C7 | 1-162-923-11 | s | CERAMIC, CHIP 47PF 5% 50V |
| C8 | 1-162-923-11 | s | CERAMIC, CHIP 47PF 5% 50V |
| C9 | 1-162-970-11 | s | CERAMIC, CHIP 0.01uF 10% 25V |
| C10 | 1-135-180-21 | s | TANTALUM 3.3uF 20% 6.3V |
| C11 | 1-164-156-11 | s | CERAMIC 0.1uF 25V |
| C12 | 1-164-156-11 | s | CERAMIC 0.1uF 25V |
| C13 | 1-135-211-11 | s | TANTALUM 6.8uF 20% 6.3V |
| C14 | 1-164-156-11 | s | CERAMIC 0.1uF 25V |
| C15 | 1-135-216-11 | s | TANTALUM 10uF 20% 10V |
| C16 | 1-162-927-11 | s | CERAMIC, CHIP 100PF 5% 50V |
| C17 | 1-135-163-21 | s | TANTALUM 47uF 20% 4V |
| C18 | 1-135-161-21 | s | TANTALUM, CHIP 22uF 10% 10V |
| C19 | 1-135-163-21 | s | TANTALUM 47uF 20% 4V |
| C20 | 1-135-179-21 | s | TANTALUM 2.2uF 20% 16V |
| C21 | 1-164-156-11 | s | CERAMIC 0.1uF 25V |
| C22 | 1-135-211-11 | s | TANTALUM 6.8uF 20% 6.3V |
| C23 | 1-164-156-11 | s | CERAMIC 0.1uF 25V |
| C24 | 1-164-156-11 | s | CERAMIC 0.1uF 25V |
| CN1 | 1-568-363-41 | s | CONNECTOR, 10P FEMALE |
| CN2 | 1-568-362-41 | s | CONNECTOR, 6P FEMALE |
| D1 | 8-719-800-76 | s | DIODE 1SS226 |
| IC1 | 8-759-941-40 | s | IC CXD1084Q-W |
| IC2 | 8-759-009-02 | s | IC MC14046BF |
| IC3 | 8-759-032-01 | s | IC MC74HC00AF |
| IC4 | 8-759-234-20 | s | IC TC7S08F |
| IC5 | 8-759-209-57 | s | IC TC4S69F |
| IC6 | *8-759-234-77 | s | IC TC4S66F |
| IC7 | *8-759-234-77 | s | IC TC4S66F |
| | *DELETED | | Ser. No. 15751 and up for XC-73<br>Ser. No. 405151 and up for XC-73CE<br>Ser. No. 63901 and up for XC-75<br>Ser. No. 53701 and up for XC-75CE |
| IC8 | 8-759-234-77 | s | IC TC4S66F |
| IC9 | 8-759-234-77 | s | IC TC4S66F |
| L1 | 1-412-006-31 | s | INDUCTOR CHIP 10UH |
| L2 | 1-412-006-31 | s | INDUCTOR CHIP 10UH |
| L3 | 1-412-796-41 | s | INDUCTOR 47UH<br>Ser. No. 10001 to 11500 for XC-75<br>Ser. No. 10001 to 10600 for XC-75CE |
| | 1-412-029-11 | ◎ | INDUCTOR, CHIP 10UH<br>Ser. No. 10001 and up for XC-73<br>Ser. No. 400001 and up for XC-73CE<br>Ser. No. 11501 and up for XC-75<br>Ser. No. 10601 and up for XC-75CE |
| Q1 | 8-729-117-16 | s | TRANSISTOR 2SA1611-M6 |
| Q2 | 8-729-117-16 | s | TRANSISTOR 2SA1611-M6 |

(SG-199 BOARD)

| Ref. No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| Q3 | 8-729-117-16 | s | TRANSISTOR 2SA1611-M6 |
| Q4 | 8-729-117-32 | s | TRANSISTOR 2SC4177 |
| Q5 | 8-729-427-74 | s | TRANSISTOR XP4601 |
| R1 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R2 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R3 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R4 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R5 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R6 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R7 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R8 | 1-216-821-11 | s | METAL, CHIP 1K 5% 1/16W |
| R9 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R10 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R11 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R12 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R13 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R14 | 1-216-813-11 | s | METAL, CHIP 220 5% 1/16W<br>Ser. No. 10001 to 15750 for XC-73<br>Ser. No. 400001 to 405150 for XC-73CE<br>Ser. No. 10001 to 63900 for XC-75<br>Ser. No. 10001 to 53700 for XC-75CE |
| | 1-216-819-11 | s | METAL, CHIP 680 5% 1/16W<br>Ser. No. 15751 and up for XC-73<br>Ser. No. 405151 and up for XC-73CE<br>Ser. No. 63901 and up for XC-75<br>Ser. No. 53701 and up for XC-75CE |
| R15 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R16 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W (for XC-73/75) |
| R17 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W<br>Ser. No. 10001 to 11270 for XC-73<br>Ser. No. 400001 to 400300 for XC-73CE<br>Ser. No. 10001 to 31800 for XC-75<br>Ser. No. 10001 to 17700 for XC-75CE |
| | 1-216-821-11 | s | METAL, CHIP 1K 5% 1/16W<br>Ser. No. 11271 and up for XC-73<br>Ser. No. 400301 and up for XC-73CE<br>Ser. No. 31801 and up for XC-75<br>Ser. No. 17701 and up for XC-75CE |
| R18 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R19 | 1-216-809-11 | s | METAL, CHIP 100 5% 1/16W |
| R20 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R21 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R22 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W (for XC-73CE/75CE) |
| R23 | 1-216-849-11 | s | METAL, CHIP 220K 5% 1/16W |
| R24 | 1-216-835-11 | s | METAL, CHIP 15K 5% 1/16W |
| R25 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R26 | 1-216-833-11 | s | METAL, CHIP 10K 5% 1/16W |
| R27 | 1-216-849-11 | s | METAL, CHIP 220K 5% 1/16W |
| R28 | 1-216-843-11 | s | METAL, CHIP 68K 5% 1/16W |
| R29 | 1-216-821-11 | s | METAL, CHIP 1K 5% 1/16W |
| R30 | 1-216-839-11 | s | METAL, CHIP 33K 5% 1/16W |
| R31 | 1-216-829-11 | s | METAL, CHIP 4.7K 5% 1/16W |
| R32 | 1-216-839-11 | s | METAL, CHIP 33K 5% 1/16W |
| R33 | 1-216-844-11 | s | METAL, CHIP 82K 5% 1/16W |
| R34 | 1-216-022-00 | s | METAL, CHIP 75 5% 1/10W |

(SG-199 BOARD)

| Ref. No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| R35 | 1-216-022-00 | s | METAL, CHIP 75 5% 1/10W |
| R36 | 1-216-829-11 | s | METAL, CHIP 4.7K 5% 1/16W |
| R37 | 1-216-825-11 | s | METAL, CHIP 2.2K 5% 1/16W |
| R38 | 1-216-821-11 | s | METAL, CHIP 1K 5% 1/16W |
| R39 | 1-216-849-11 | s | METAL, CHIP 220K 5% 1/16W |
| R40 | *1-216-821-11 | s | METAL, CHIP 1K 5% 1/16W |
| R41 | *1-216-821-11 | s | METAL, CHIP 1K 5% 1/16W |
| | *ADD | | Ser.No. 15751 and up for XC-73 |
| | | | Ser.No. 405151 and up for XC-73CE |
| | | | Ser.No. 63901 and up for XC-75 |
| | | | Ser.No. 53701 and up for XC-75CE |
| S1 | 1-571-120-11 | s | SWITCH, SLIDE |
| | | | Ser.No. 10001 to 15750 for XC-73 |
| | | | Ser.No. 400001 to 405150 for XC-73CE |
| | | | Ser.No. 10001 to 63900 for XC-75 |
| | | | Ser.No. 10001 to 53700 for XC-75CE |
| | 1-572-972-21 | s | SWITCH, CHIP |
| | | | Ser.No. 15751 and up for XC-73 |
| | | | Ser.No. 405151 and up for XC-73CE |
| | | | Ser.No. 63901 and up for XC-75 |
| | | | Ser.No. 53701 and up for XC-75CE |
| S2 | 1-571-120-11 | s | SWITCH, SLIDE |
| S3 | 1-571-120-11 | s | SWITCH, SLIDE |

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FRAME
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| Ref. No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| 1pc | 1-547-185-31 | o | FILTER, INFRARED CUT |
| 1pc | 1-642-810-11 | s | WIRE, FLEXIBLE CARD, 20P, HN-179 |
| CN101 | 1-562-381-00 | s | CONNECTOR, 12P MALE "DC IN/SYNC" |
| CN102 | 1-580-724-21 | s | CONNECTOR, BNC "VIDEO OUT" |
| CN103 | 1-562-222-21 | s | CONNECTOR 6P FEMALE "LENS" |

# JUNCTION BOX
# JB-77

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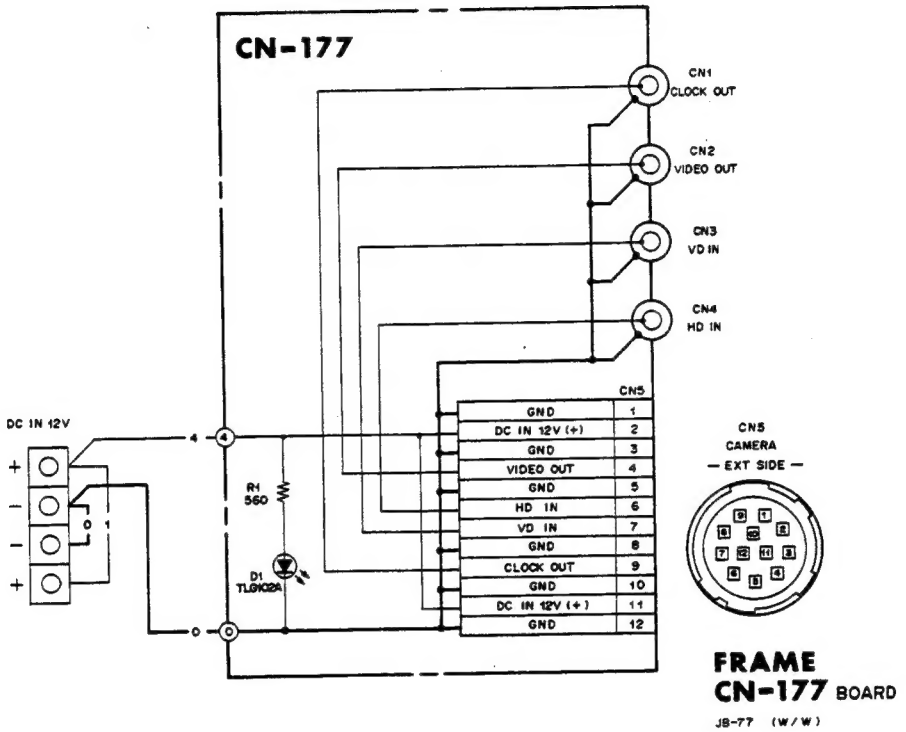
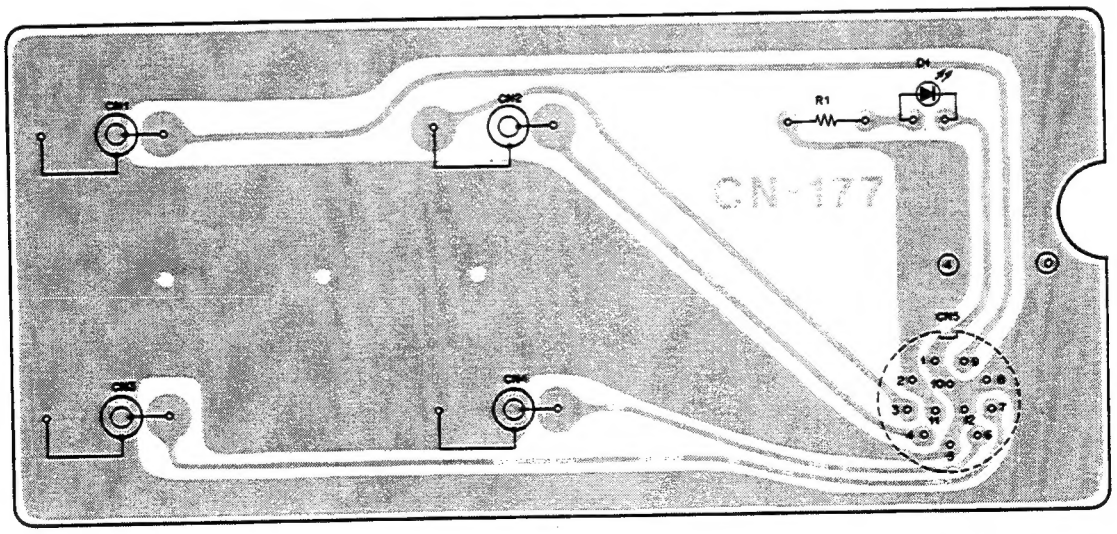
# SCHEMATIC DIAGRAM & MOUNTING DIAGRAM

## JUNCTION BOX(JB-77)




**FRAME**
**CN-177** BOARD
JB-77 (W/W)




**CN-177** BOARD
— SOLDERING SIDE —
1-621-376-11
JB-77 (W/W)

## ELECTRICAL PARTS LIST

| Ref.No. or Q'ty | Part No. | SP | Description |
|---|---|---|---|
| | | | **CN-177 BOARD** |
| 1pc | 1-621-376-11 | o | PRINTED CIRCUIT BOARD, CN-177 |
| D1 | 8-719-800-33 | s | DIODE TLG102A |
| R1 | 1-249-414-11 | s | RES, CARBON 560 5% 1/6W |
| | | | **FRAME** |
| 1pc | 1-537-047-11 | o | TERMINAL BOARD "DC IN +12V" |
| CN1 | 1-562-382-00 | s | CONNECTOR, BNC "CLOCK OUT" |
| CN2 | 1-562-382-00 | s | CONNECTOR, BNC "VIDEO OUT" |
| CN3 | 1-562-382-00 | s | CONNECTOR, BNC "VD IN" |
| CN4 | 1-562-382-00 | s | CONNECTOR, BNC "HD IN" |
| CN5 | 1-562-221-31 | s | CONNECTOR, 12P FEMALE "CAMERA" |

# STANDARD LENS

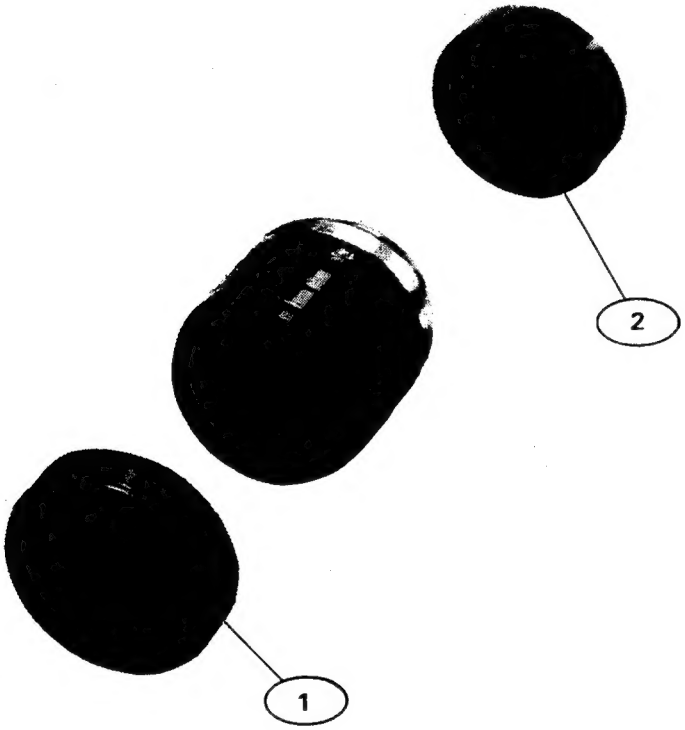
# VCL-08YM

# VCL-12YM

# VCL-16Y-M

## STANDARD LENS (VCL-08YM/VCL-12YM/VCL-16Y-M)

| No. | Part No. | SP | Description |
|---|---|---|---|
| 1 | 3-707-313-01 | o | CAP, FRONT |
| 2 | 3-707-314-01 | o | CAP, REAR |




(PHOTO: VCL-16Y-M)